APPENDIX B

Z86017 / Z16017 ELECTRICAL CHARACTERISTICS AND TIMING

B.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Unit	Min. Value	Max. Value
Supply Voltage	V_{DD}	V	–0.5	7.0
Input Voltage	V_I	V	–0.5	V_{DD} + 0.5
Output Voltage	V_O	V	–0.5	V_{DD} + 0.5
Storage Temperature	T_{STG}	C	–40	+125
Temperature Under Bias	T_{BIAS}	C	–25	+85

B.2 DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V ±10%

		T_A = 0°C to +70°C		Typical			
Sym.	Parameter	Min.	Max.	at 25°C	Units	Conditions	Notes
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC}		V		
V_{IL}	Input Low Voltage	–0.3	0.1 V_{CC}		V		
V_{OH}	Output High Voltage	1.8			V	I_{OH} = 4 mA	
V_{OH}	Output High Voltage	V_{CC} – 100 mV			V	I_{OH} =100 µA	
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = 4 mA	
V_{RH}	Reset Input High Voltage	0.8 V_{CC}	V_{CC}		V		
V_{RI}	Reset Input Low Voltage	–0.3	0.1 V_{CC}		V		
I_{IL}	Input Leakage	–2	2		µA	Test at 0V, V_{CC}	
I_{OL}	Output Leakage	–2	2		µA	Test at 0V, V_{CC}	
I_{IR}	Reset Input Current		–80		µA	V_{RL} = 0V	
I_{CC}	Supply Current		4	3	mA	@ 20 MHz	[1]
I_{CC1}	Standby Current		300	250	µA		[2]

Notes:
[1] All inputs driven to 0V, V_{cc} and outputs floating.
[2] EN_Pads Bit Set, PC_MCLK = 0, EE_SK=0

V_{CC} = 5.0V ±10%

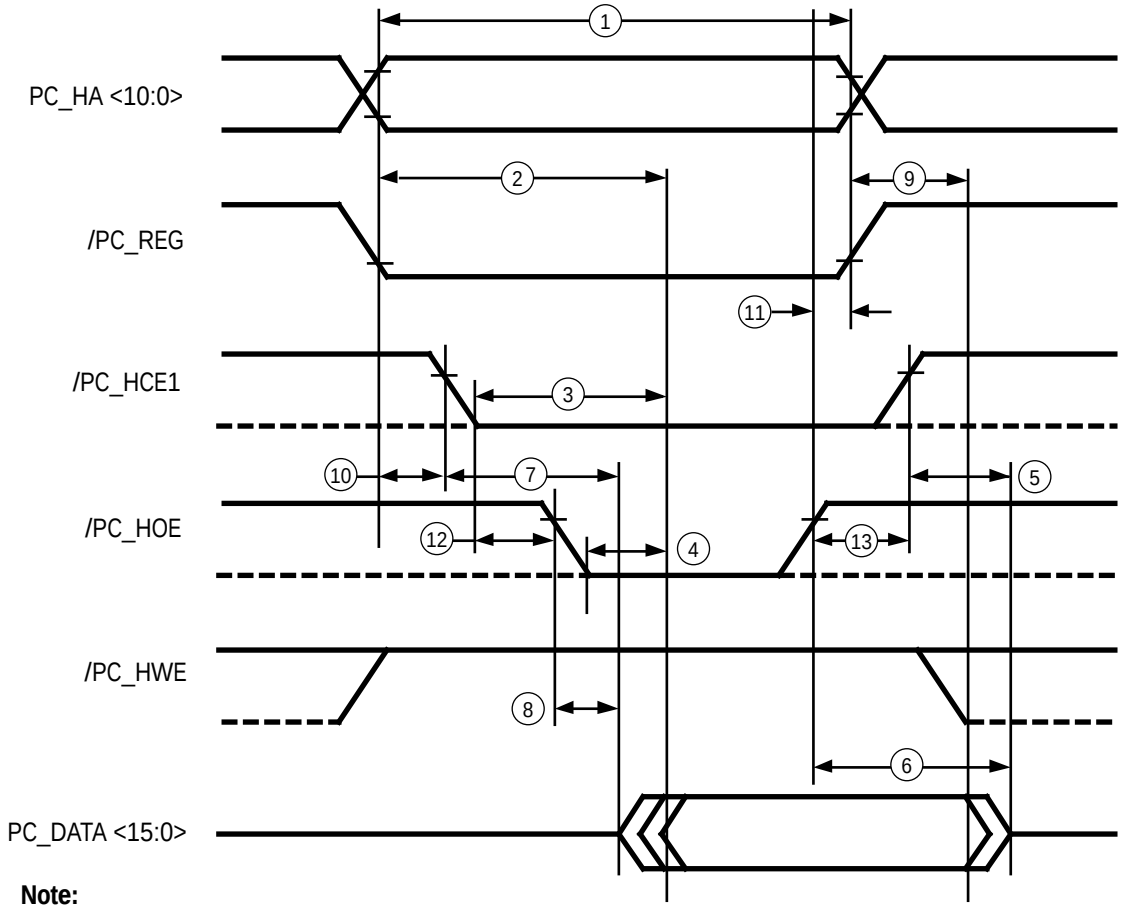
Sym.	Parameter	T_A = 0°C to +70°C Min.	Max.	Typical at 25°C	Units	Conditions	Notes
V_{IH}	Input High Voltage	2.0	V_{CC}		V		
V_{IL}	Input Low Voltage	–0.3	0.8		V		
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –6 mA	
V_{OH}	Output High Voltage	V_{CC} –100 mV			V	I_{OH} = 100 µA	
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = 6 mA	
V_{RH}	Reset Input High Voltage	3.8	V_{CC}		V		
V_{RI}	Reset Input Low Voltage	–0.3	0.8		V		
I_{IL}	Input Leakage	–2	2		µA	Test at 0V, V_{CC}	
I_{OL}	Output Leakage	–2	2		µA	Test at 0V, V_{CC}	
I_{IR}	Reset Input Current		–80		µA	V_{RL} = 0V	
I_{CC}	Supply Current		5	4	mA	@ 20 MHz	[1]
I_{CC1}	Standby Current		350	300	µA		[2]

Notes:
[1] All inputs driven to 0V, or V_{cc} and outputs floating.
[2] EN_Pads bit set, PC_MCLK = 0, EE_SK = 0

B.3 INTERNAL ATTRIBUTE MEMORY TIMING

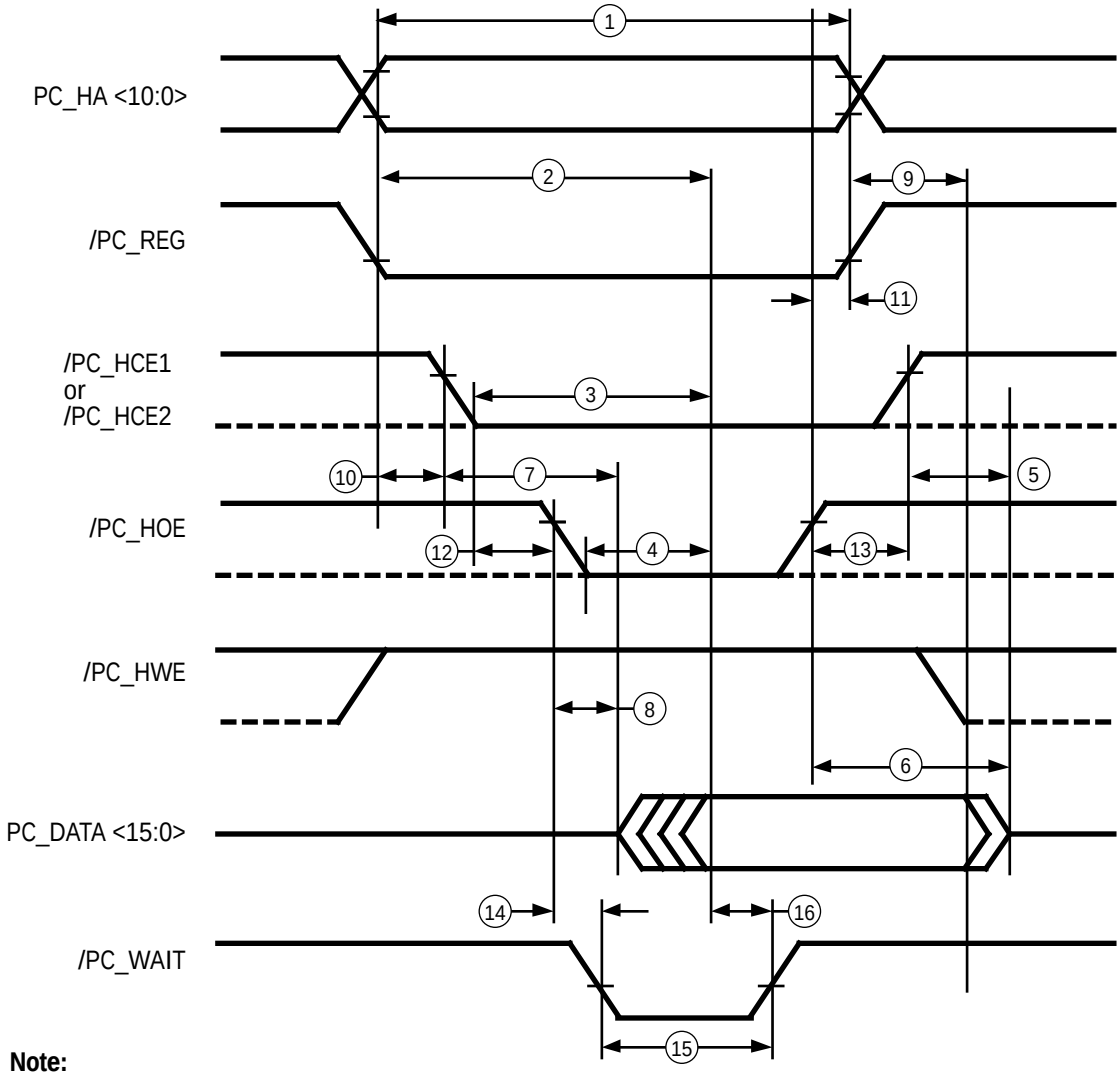
(Speed Version: 300 ns)

No.	Symbol	Parameter	Min.	Max.	Units
1	TcR	Read Cycle Time	300		ns
2	TaA	Address Access Time		300	ns
3	TaCE	Card Enable Time		300	ns
4	TaOE	Output Enable Access Time		150	ns
5	TdisCE	Output Disable Time from CE		100	ns
6	TdisOE	Output Disable Time from OE		100	ns
7	TenCE	Output Enable Time from CE	5		ns
8	TenOE	Output Enable Time from OE	5		ns
9	TvA	Data Valid from Address Change	0		ns
10	TsuA	Address Setup Time	30		ns
11	ThA	Address Hold Time	20		ns
12	TsuCE	Card Enable Setup Time	0		ns
13	ThCE	Card Enable Hold Time	20		ns
14	TvWToe	Wait Valid from OE		35	ns
15	TwWT	Wait Pulse Width		12	µs
16	TvWT	Data Setup for Wait Released	0		ns



Note:
/PC_REG is active Low for Attribute Memory reads only.

Figure B-1. PCMCIA Read Memory Timing, No Wait States



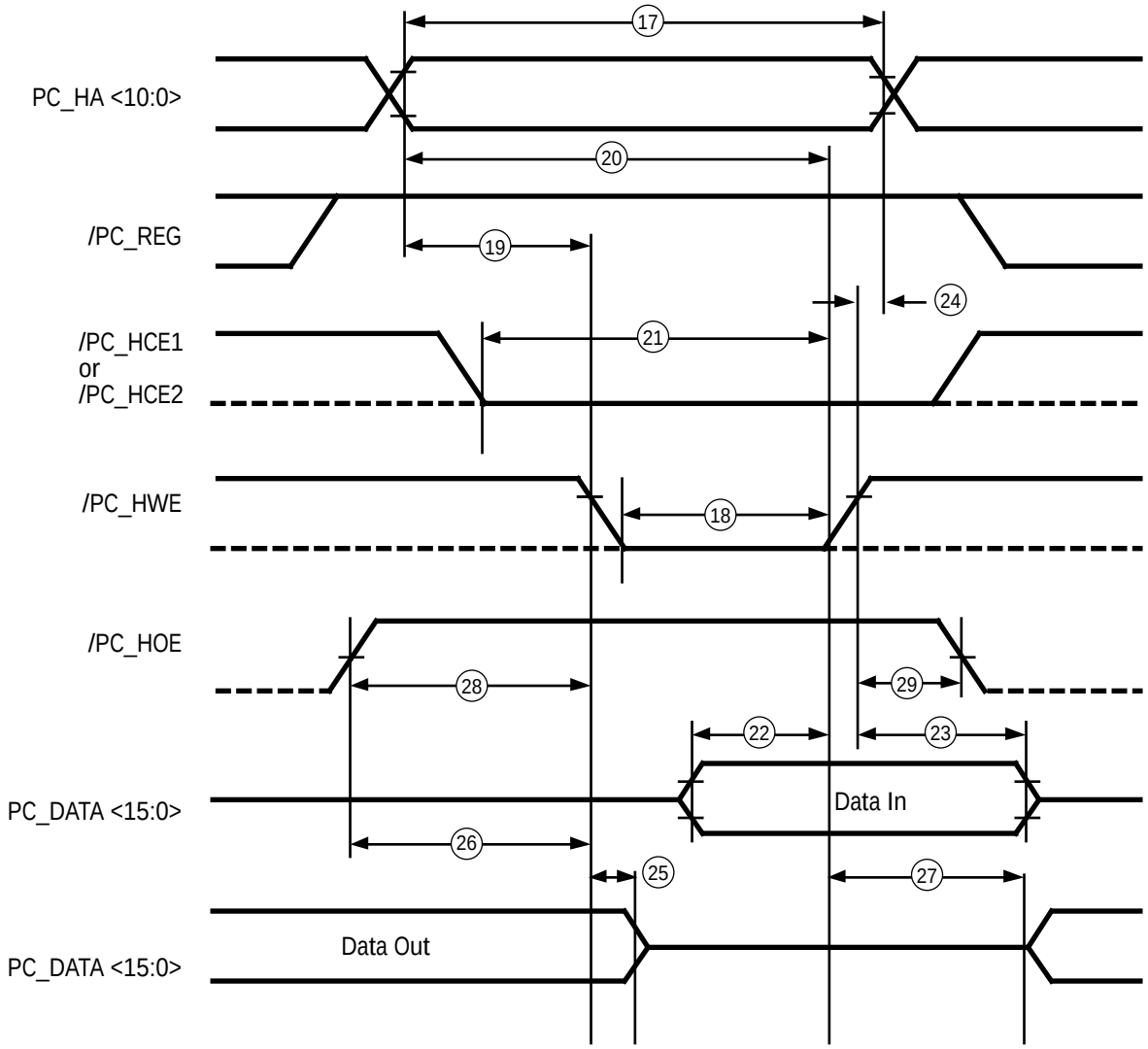
Note:
/PC_REG is active Low for Attribute Memory reads only.

Figure B-2. PCMCIA Read Memory Timing, Wait State Enabled

2.4 PCMCIA MEMORY WRITE TIMING

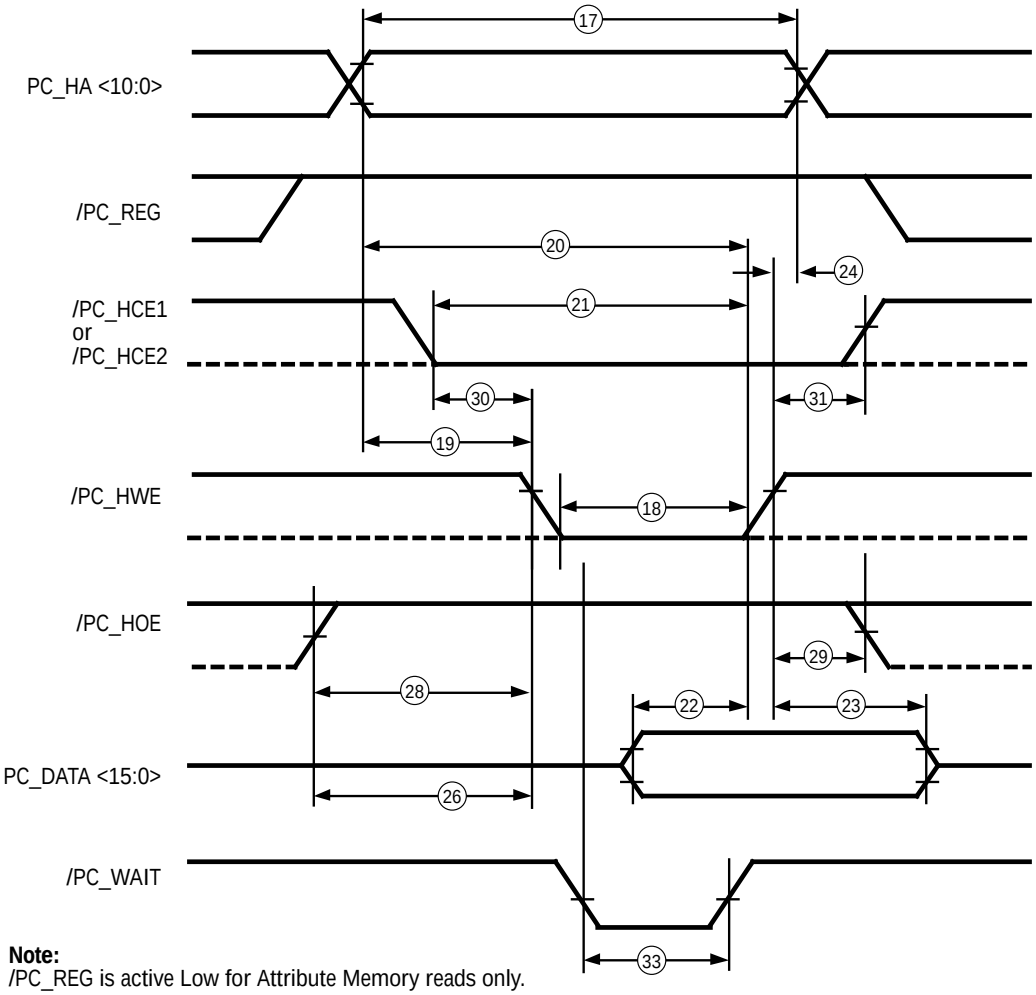
No.	Symbol	Parameter	200 ns Min.	200 ns Max.	150 ns Min.	150 ns Max.	100 ns Min.	100 ns Max.	Units
17	TcW	Write Cycle Time	200		150		100		ns
18	TwWE	Write Pulse Width	120		80		60		ns
19	TsuA	Address Setup Time	20		20		10		ns
20	TsuAwe	Address Setup Time for WE	140		100		70		ns
21	TsuCwe	Card Enable Setup Time for WE	140		100		70		ns
22	TsuDwe	Data Setup Time for WE	60		50		40		ns
23	ThD	Data Hold Time	30		20		15		ns
24	TrecWE	Write Recover Time	30		20		15		ns
25	TdisOwe	Output Disable Time from WE		90		75		50	ns
26	TdisOE	Output Disable Time from OE		90		75		50	ns
27	TenWE	Output Enable Time from WE	5		5		5		ns
28	TsuCwe	Output Enable Setup from WE	10		10		10		ns
29	ThCwe	Card Enable Hold from WE	10		10		10		ns
30	TsuCE	Card Enable Setup Time	0		0		0		ns
31	ThCE	Card Enable Hold Time	20		20		15		ns
32	TvWTwe	Wait Valid from WE		35		35		35	ns
33	TwWT	Wait Pulse Width		12		12		12	µs
34	TvWT	WE High from Wait Released	0		0		0		ns

2.4 PCMCIA MEMORY WRITE TIMING (Continued)



Note: PC_REG is active Low for Attribute Memory reads only.

Figure B-3. PCMCIA Write Memory Timing, No Wait States



Note:
/PC_REG is active Low for Attribute Memory reads only.

Figure B-4. PCMCIA Write Memory Timing, Wait State Enabled

2.5 I/O READ TIMING SPECIFICATION

No.	Symbol	Parameter	Min.	Max.	Units
35	TdIORD	Data Delay After IORD	100		ns
36	ThIORD	Data Hold Following IORD	0		ns
37	twIORD	IORD Width Time	165		ns
38	TsuAiord	Address Setup Before IORD	70		ns
39	ThAiord	Address Hold Following IORD	20		ns
40	TsuCEiord	CE Setup Before IORD	5		ns
41	ThCEiord	CE Hold Following IORD	20		ns
42	TsuRGiord	REG Setup Before IORD	5		ns
43	ThRGiord	REG Hold Following IORD	0		ns
44	TdIPKiord	INPACK Delay to IORD	0	45	ns
45	TdIPKiord	INPACK Delay from IORD		45	ns
46	TdIOISad	IOIS16 Delay from Address		35	ns
47	TdIOISadr	IOIS16 Delay Rise from Address		35	ns
48	TdWiord	Wait Delay from IORD		35	ns
49	TdWTr	Data Delay from Wait Rising		35	ns
50	TwWT	Wait Width Time		12	µs

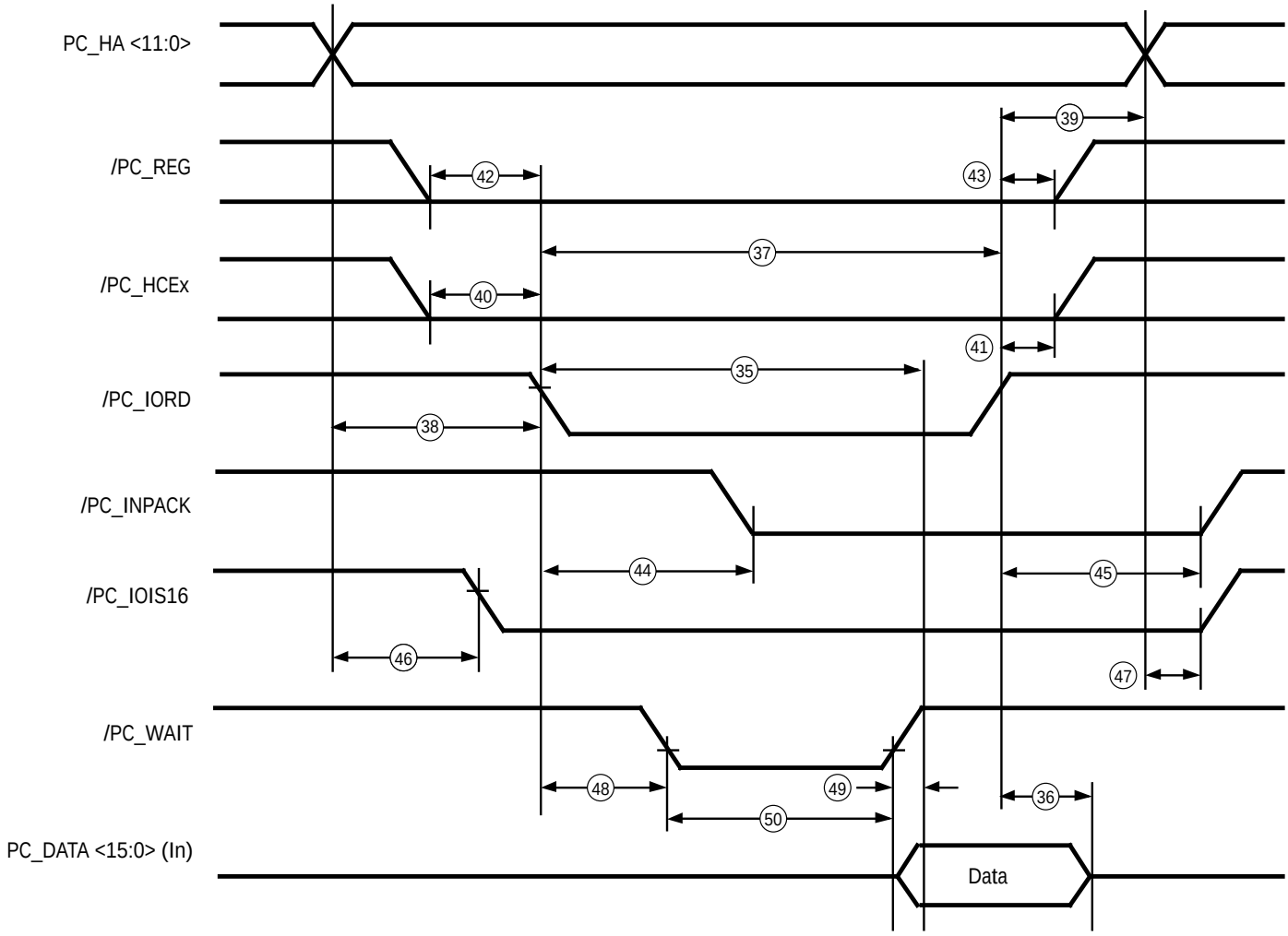


Figure B-5. I/O Read Timing

2.6 I/O WRITE TIMING SPECIFICATION

No.	Symbol	Parameter	Min.	Max.	Units
51	TsuIOWR	Data Setup before IOWR	60		ns
52	ThIOWR	Data Hold after IOWR	30		ns
53	TwIOWR	IOWR Width Time	165		ns
54	TsuAiowr	Address Setup to IOWR	70		ns
55	ThAiowr	Address Hold after IOWR	20		ns
56	TsuCEiowr	CE Setup before IOWR	5		ns
57	ThCEiowr	CE Hold after IOWR	20		ns
58	TsuRGiowr	REG Setup before IOWR	5		ns
59	ThRGiowr	REG Hold after IOWR	0		ns
60	TdIOISadr	IOIS16 Delay Falling from Address		35	ns
61	TIdIOISadr	IOIS16 delay Rising from Address		35	ns
62	TdWTiowr	Wait Delay Falling from IOWR		35	ns
63	TwWT	Wait Width Timing		12	µs

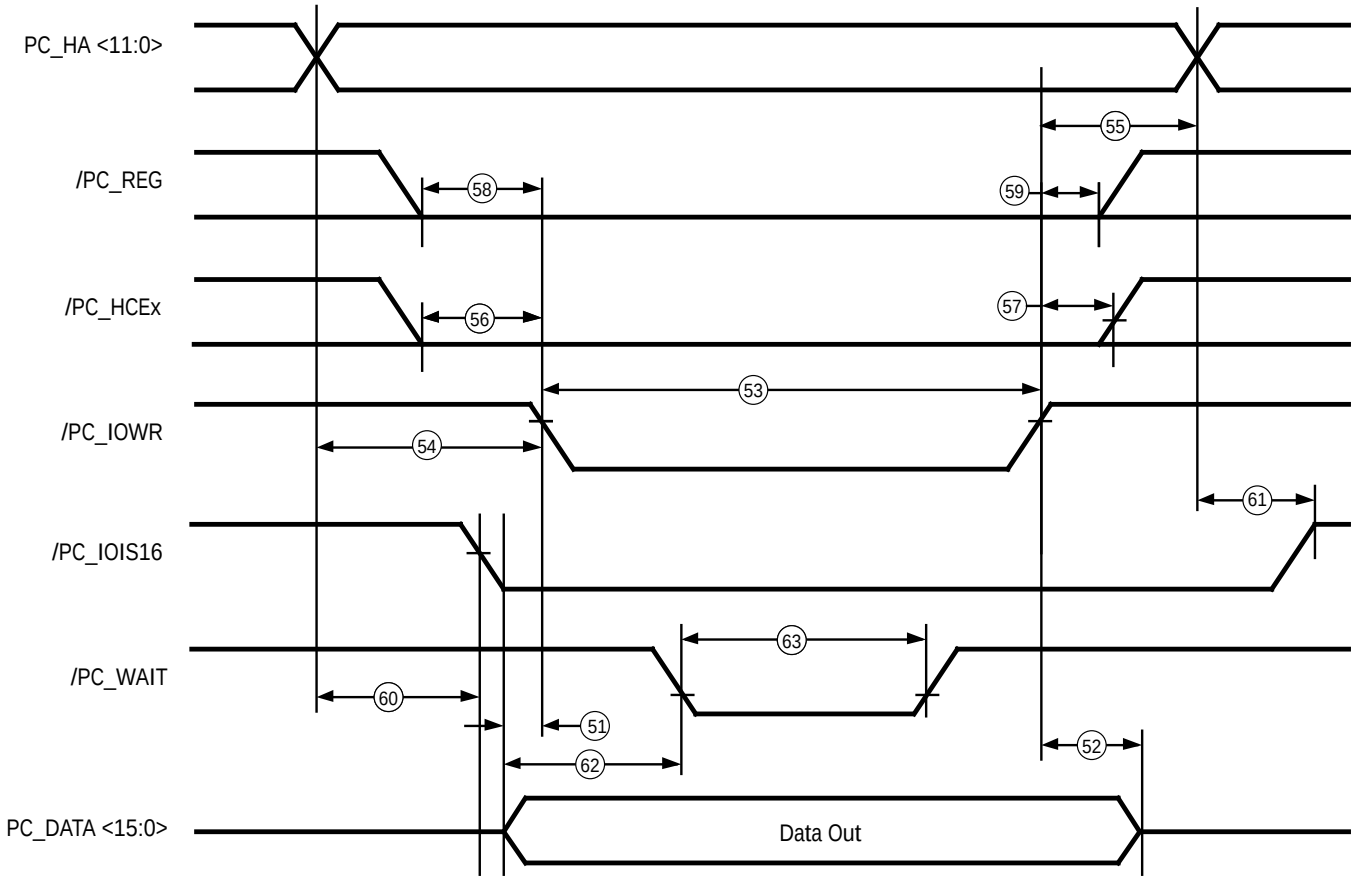


Figure B-6. I/O Write Timing

2.7 SKEW TIMING BETWEEN PCMCIA AND ATA/IDE OR PERIPHERAL BUS

No.	Symbol	Parameter	Min.	Max.	Units
64	TskADR	Address Skew	0	25	ns
65	TskI/Of	I/O Fall Skew	0	25	ns
66	TskI/Or	I/O Rise Skew	0	25	ns
67	TskMEMf	Mem Fall Skew	0	25	ns
68	TskMEMr	Mem Rise Skew	0	25	ns

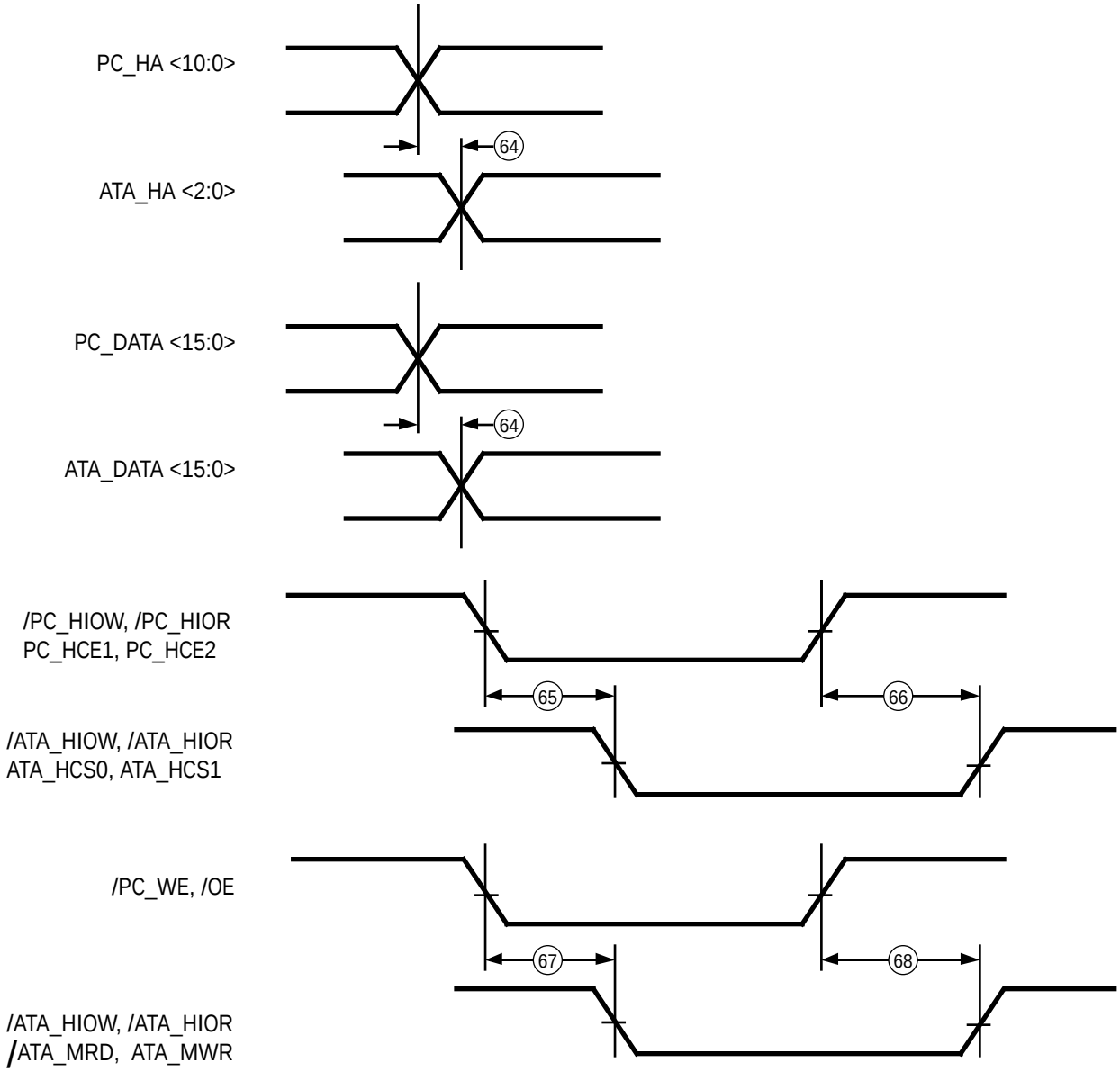


Figure B-7. Skew Timing Between PCMCIA and ATA/IDE or Peripheral Bus

2.8 017 DEVICE SLEW DELAY

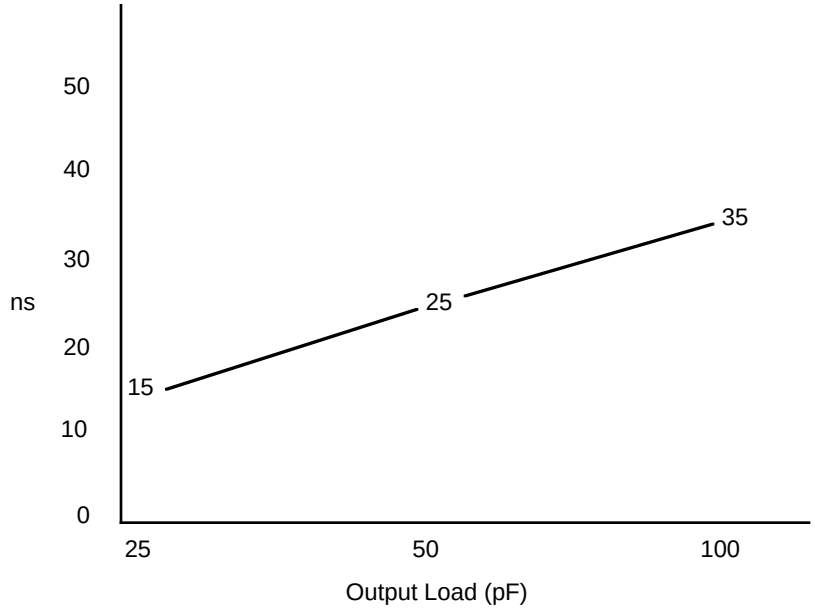


Figure B-8. 017 Slew Delay Derating Curve (Typical)

B.9 SERIAL INTERFACE TIMING

No.	Symbol	Parameter	Min.	Max.	Units
69	TpMCKin	Master Clock In Period	50		ns
70	TsuCS	CS Setup to CLK time	25		ns
71	ThCS	CS Hold after CLK	0		ns
72	ThDout	Data Hold Time	10		ns
73	TsuDout	Data Setup Time	25		ns
74	ThDin	Data Hold Time	0		ns
75	TsuDin	Data Setup Time	25		ns
76	TpCKw	Clock Period, Master	200		ns
77	TpCKs	Clock Period, Slave	200		ns

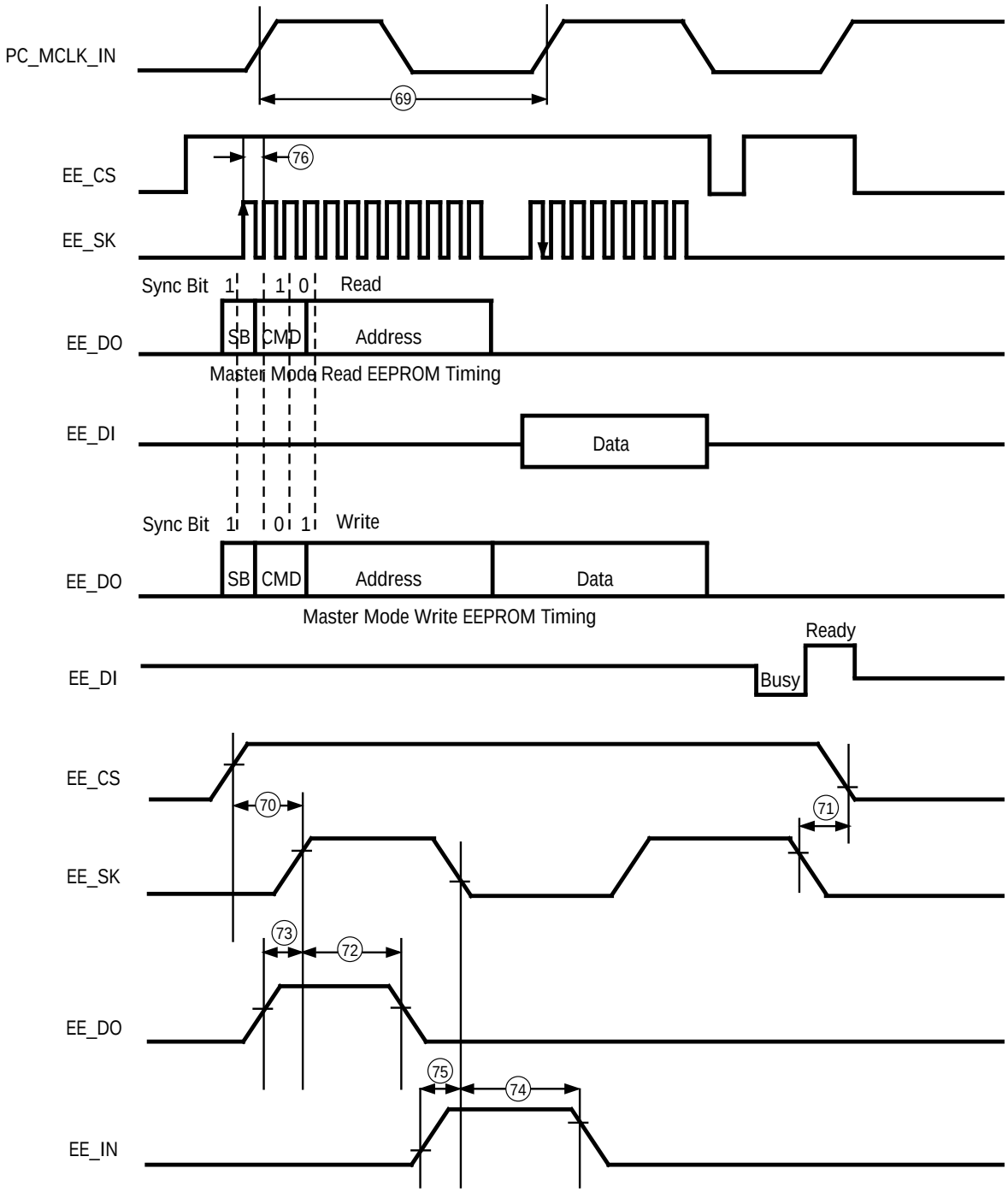
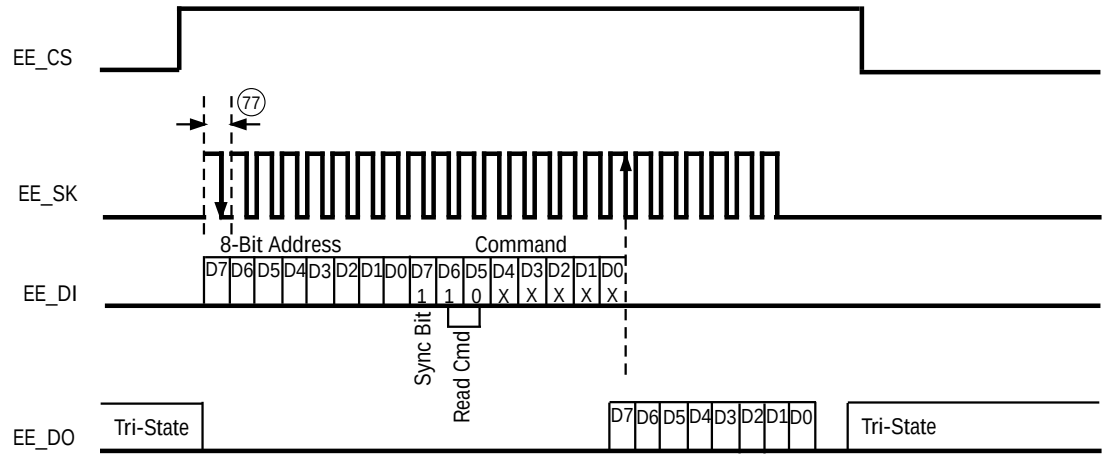
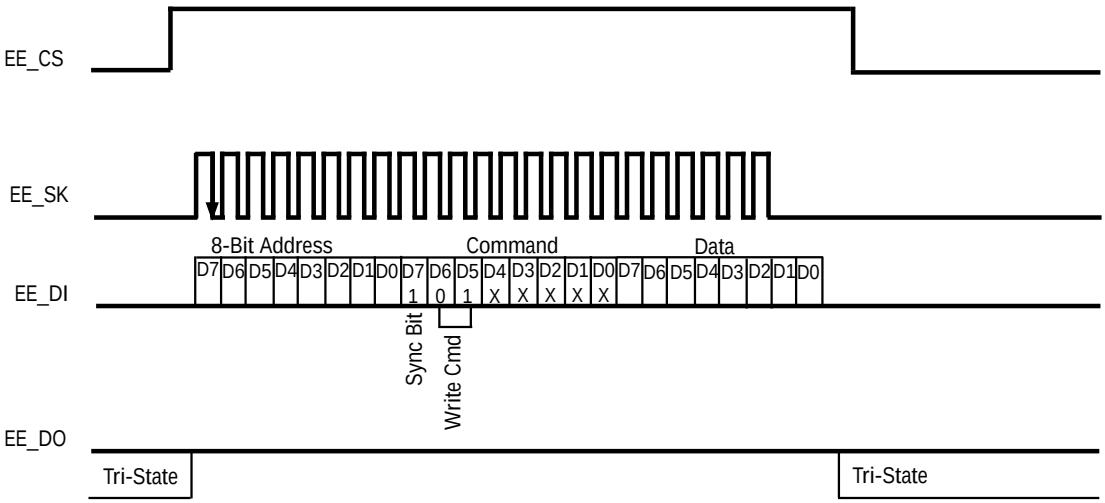


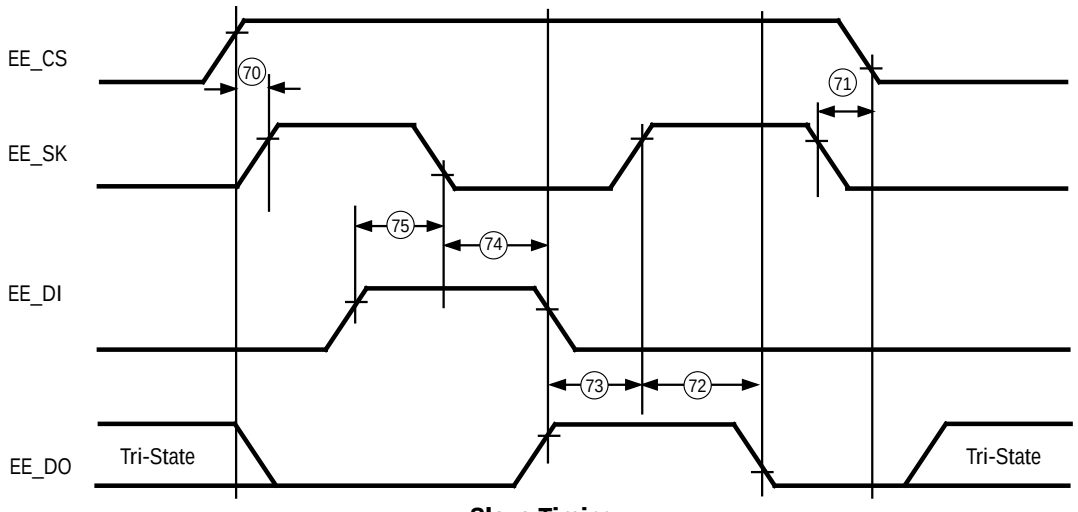
Figure B-9. Master Mode Read EEPROM Timing



Slave Read Command



Slave Write Command



Slave Timing

Figure B-10. Slave Interface Timing (Read)