CHAPTER 1
Z86017/Z16017 PCMCIA INTERFACE OVERVIEW

1.1 FEATURES

Device	RAM (Bytes)	Speed	Package
Z86017	256	20	100–Pin VQFP
Z86M17*	256	20	100–Pin VQFP
Z16017	256	20	100–Pin VQFP
Z16M17*	256	20	100–Pin VQFP

* Mirror Image Bond-Out Options

- PCMCIA Configuration Registers
- Sequencer for Programming Attribute Memory using EEPROM content, Master Mode
- Serial Peripheral Interface (SPI) Circuitry Allows Control Through the Local Microprocessor, Slave Mode
- PCMCIA to I/O Peripheral
- PCMCIA to ATA/IDE Translation
- ATA/IDE to ATA/IDE Mapping, Pass Through Mode
- Operates from a 3V to 5.5V Power Supply
- Conforms to PCMCIA Standards
- Low Power Dissipation
- Mirror Image Bond-Out Option (Z86M17/Z16M17)
- On-Chip Generation of IOIS16 in I/O Mode (Z16017)

1.2 GENERAL DESCRIPTION

The Z86017/Z16017 (017) are general-purpose PCMCIA adapter chips used on the card side of the interface. For increased versatility, “mirror image” bond-out versions, the Z86M17 and Z16M17, are also available. These chips are easily configured to allow access to all types of memory or I/O-mapping peripherals, such as Ethernet controllers, Universal Asynchronous Receiver/Transmitters (UART), modems, rotating disk memory, and so on.

The 017 can be used in a stand-alone configuration without the use of a local processor when all necessary data for Attribute Memory, Card Configuration Registers (CCR), Memory/I/O maps, and so on, are being provided by a local serial EEPROM. The serial EEPROM is read automatically using an internal EEPROM sequencer. The 017 can also be configured by a local microprocessor, when one is being used on the card.

Throughout this document, references to the 017 device applies equally to the Z86017 and Z16017, unless otherwise specified.

Notes: All Signals with a preceding front slash, /, are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

1.2 GENERAL DESCRIPTION (Continued)

The 017 can be programmed by one of two ways: an external 256 byte serial EEPROM can be connected to the serial port interface, or a microprocessor can be connected to this port to provide a higher level of control. The functional block diagram for the 017 device is shown in Figure 1-1.

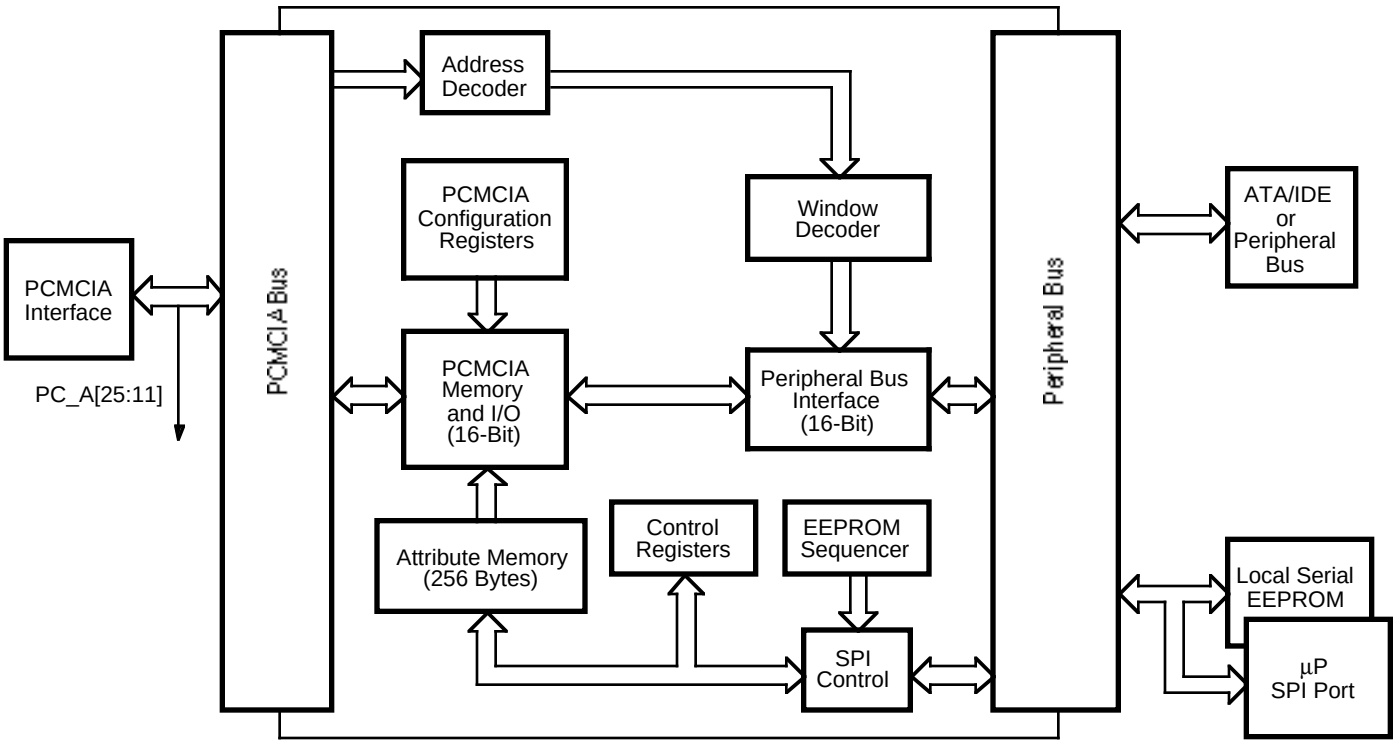

Figure 1-1. 017 Functional Block Diagram

1.2.1 Power-On Reset

The 017 defaults to the Memory Only interface as outlined in the PCMCIA specification upon deassertion of Power-On Reset (/POR). The hardware sets Busy on the PC_RDY//BSY pin and then addresses the EE_MASTER pin. If the EE_MASTER pin is unconnected or pulled High, the 017 serial interface defaults to the Master mode and an external EEPROM is required. If this pin is pulled Low, the Slave mode is selected and an external microprocessor is required to configure the 017 through the serial interface pins.

Next, the hardware addresses the /PC_ATA//HOE pin. If the /PC_ATA//HOE pin is held Low for 40 clocks (PC_MCLK_IN) after POR deassertion, the 017 is enabled for ATA/IDE to ATA/IDE pass through mode. The pass through mode is for systems that use the physical PCMCIA 68-pin connector but do not support PCMCIA protocol. If this pin is held High (/PC_ATA//HOE), the device is placed into the PCMCIA mode. The override bits in register 00H determine what mode(s) the user can support.

1.2.2 Serial Port Operation (Master) Mode

After the 017 determines that an external EEPROM is present (see Figure 1-2), the Ready/Busy pin on the PCMCIA interface is set to Busy. The 017 internal sequencer starts up and reads EEPROM address 1EH. If EEPROM address 1EH is loaded with a 1CH then the EEPROM's data is considered to be valid. After that, the internal sequencer resets its address counter back to zero. Data from EEPROM's addresses [00-2F] is read out and put into the on-board registers of the 017. The EEPROM sequencer then reads EEPROM addresses 30H to FFH and each byte is moved into the 017 on-board attribute memory addresses 00-CFH. After loading the registers and attribute memory, the sequencer completes by clearing the Ready/Busy pin on the PCMCIA interface indicating

"Ready." If EEPROM address 1EH does not contain 1CH, then the sequencer stops. The PCMCIA Ready/Busy pin stays in the Busy state, the on-board registers of the 017 remain in their default state, and attribute memory data is unknown. The user can then program the off-board EEPROM through the PCMCIA interface by means of three special registers and Busy should be ignored.

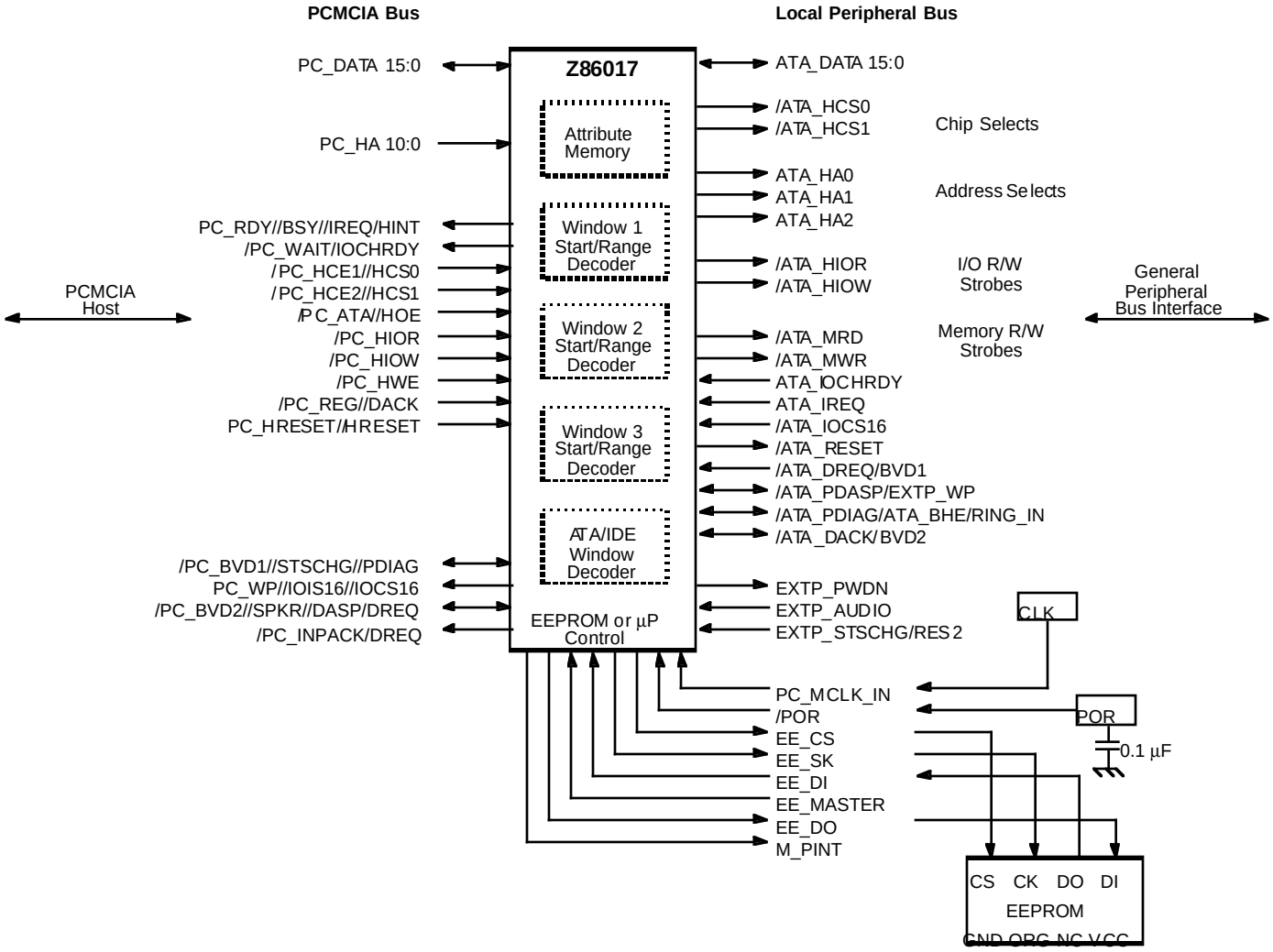

Figure 1-2. Serial Port Master Mode Control

1.2.3 Serial Port Operation (Slave) Mode

When the 017 is placed in serial port Slave mode (EE_Master signal grounded on POR), the EEPROM sequencer is disabled and the user must provide external hardware (microprocessor) with serial interface to program CCRs and Attribute Memory. Additionally, if the POR signal is deasserted, the user must provide a clock source on the PC_MCLK_IN pin in the range of 1-20 MHz.

The external hardware can program the on-board registers and the attribute memory by selecting the 017 and pulling the EE_CS pin High. The external hardware must set up the data to be sent to the 017 on the EE_DI pin and strobe the EE_SK pin. The first byte of data is the address selected by the user, the second byte is the command byte and the third byte is the data. The external hardware must provide 24 clocks in order to read or write to a location in the 017 (see B-9, Slave Timing).

In order to program the on-board attribute memory, the user must first write to it. This is accomplished by writing the address location of the attribute memory to be written to (or read) in the attribute RAM data address register at location 08H. After this step has been accomplished, the user then writes (or reads) the attribute RAM data register 09H with the data to be read or written at that location. **Note:** After reading or writing to the attribute RAM data register, the attribute RAM address register is auto-incrimented.

The following example demonstrates how to program the 017 in Slave Mode. The external user's hardware writes to register 00 and selects the clock divide by and the override mode (if needed). The READY//BUSY pin remains set to 0 to indicate BUSY, and a local µP interrupt polarity is selected. The user then programs registers 01-05, followed by registers 0AH-2FH. After which, the user writes to the attribute memory by setting the address in the address register 08H and in the loop on data register 09H with the user's attribute memory data. The user completes the operation by writing back to register 00 to clear the READY//READY status.

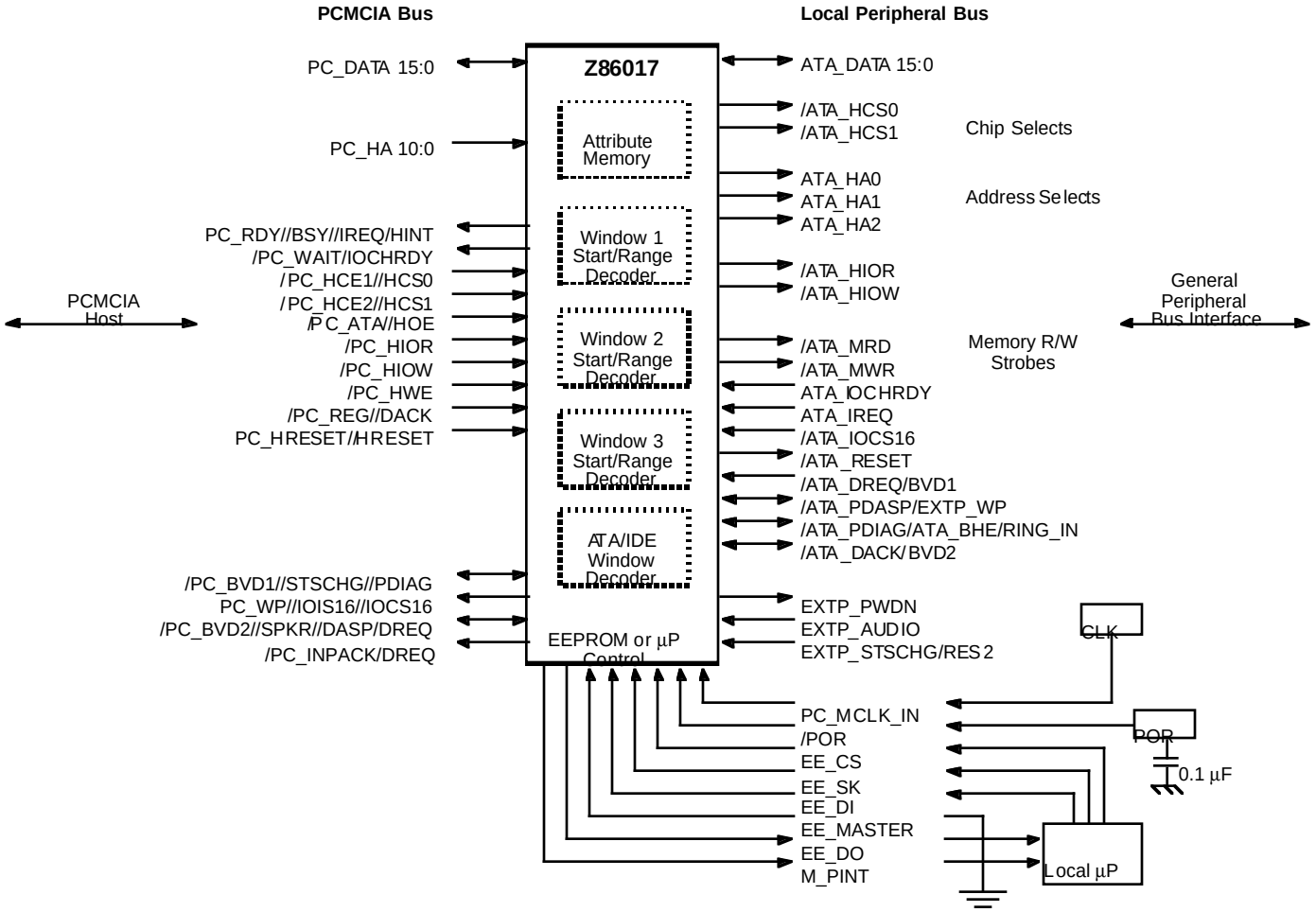

Figure 1-3. Serial Port Slave Mode Control

1.2.4 EEPROM Programming Through the PCMCIA Interface

The 017 can be used to program the serial EEPROM through the PCMCIA interface. EEPROM programming is accomplished by means of three special registers that are accessed identically to the CCR registers as defined by the PCMCIA specification (Figure 1-4). These registers are fixed at addresses 7F0, 7F2, and 7F4. The host software can read and write each byte of the EEPROM through these registers and configure the 017 device. After the host writes new values to the EEPROM through these registers, the new values are loaded into the 017 upon Power-On Reset (/POR). **Note**: The values written to register 05H will offset the CCR registers and the three special EEPROM programming registers on the next POR.

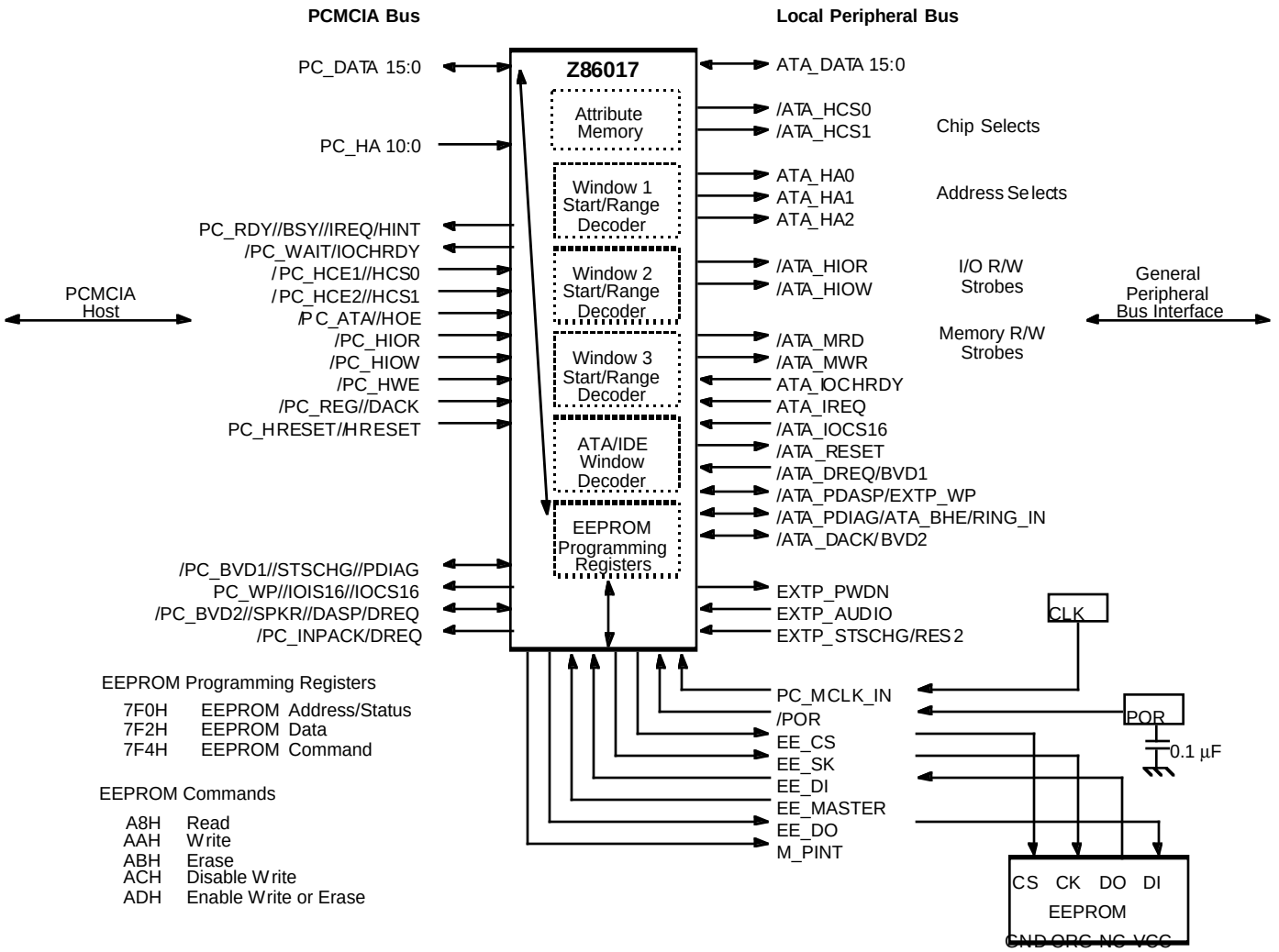

Figure 1-4. EEPROM Programming Through the PCMCIA Interface

1.2 GENERAL DESCRIPTION (Continued)

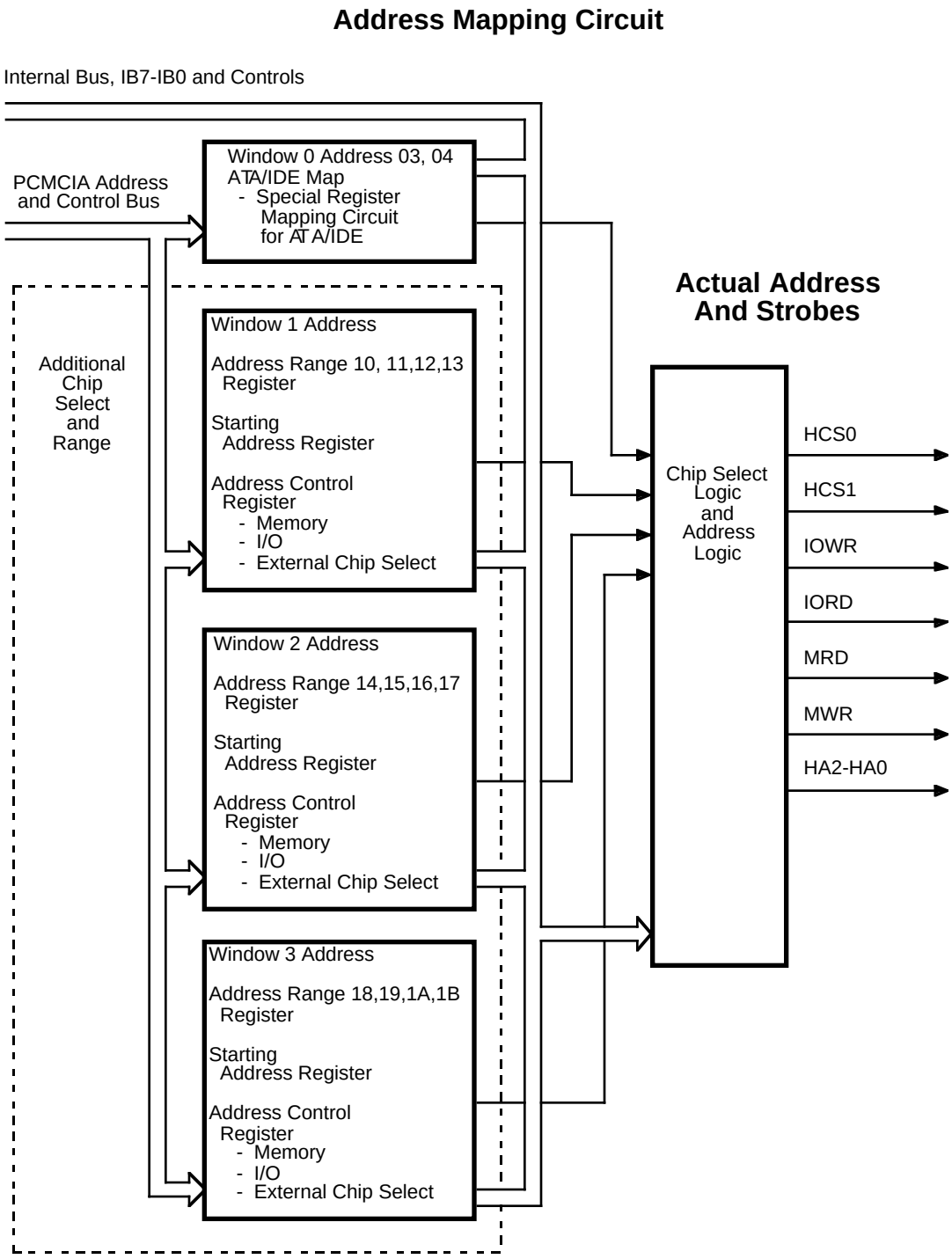

Figure 1-5. Connection Block Diagram

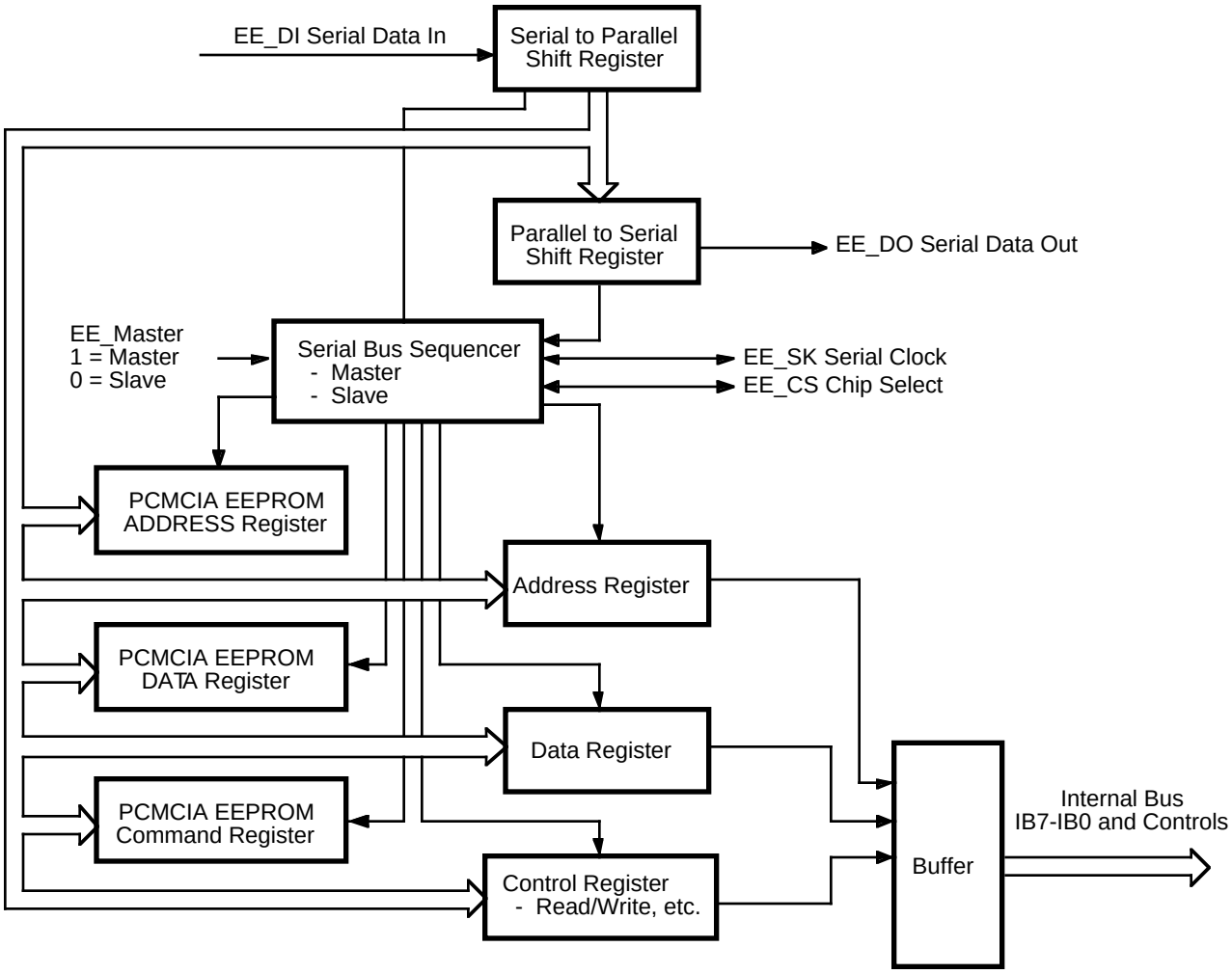

Figure 1-6. Serial Interface Diagram

1.2 GENERAL DESCRIPTION (Continued)

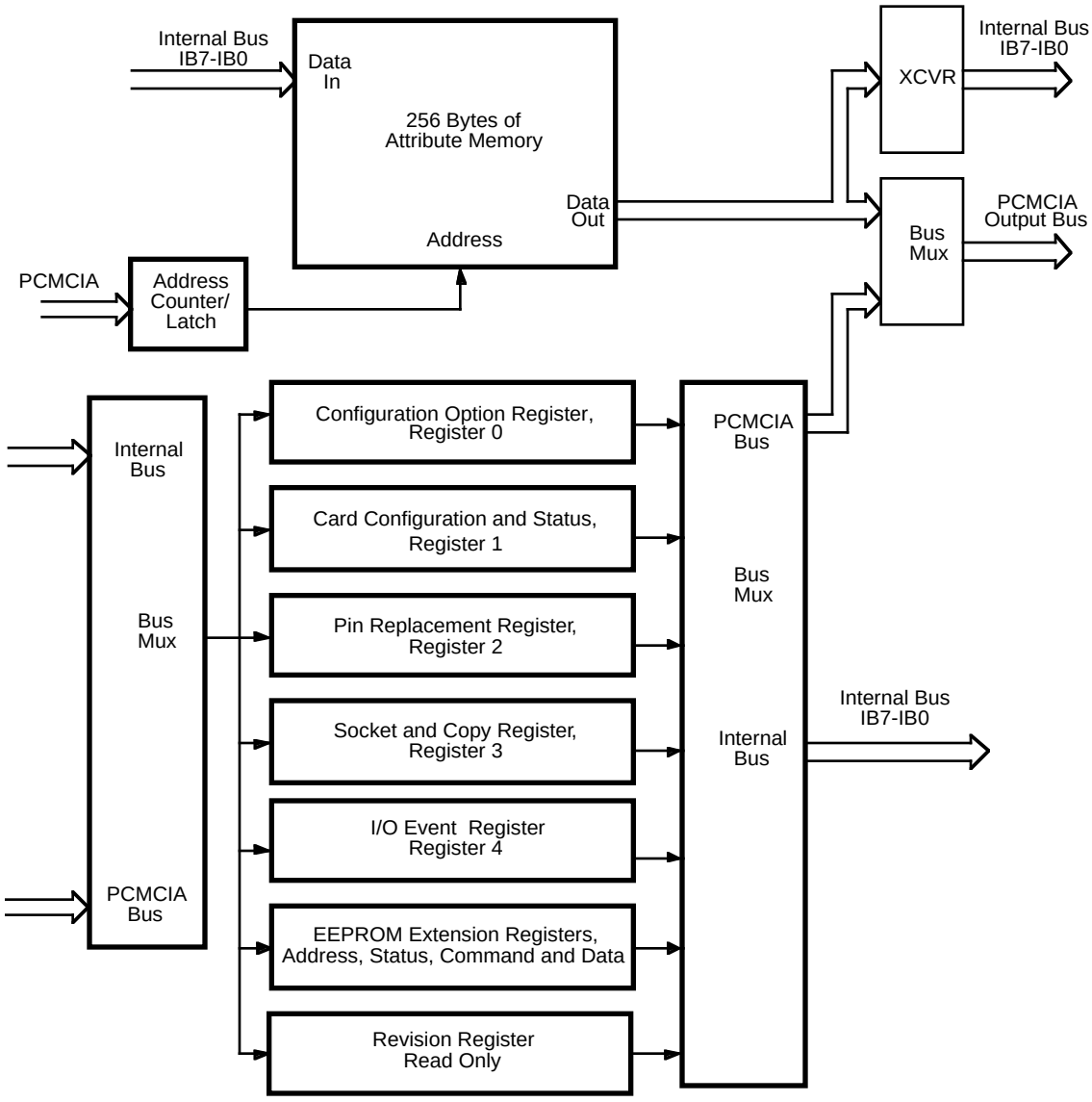

Figure 1-7. Attribute and Configuration Memory Diagram

1.3 PIN DESCRIPTION

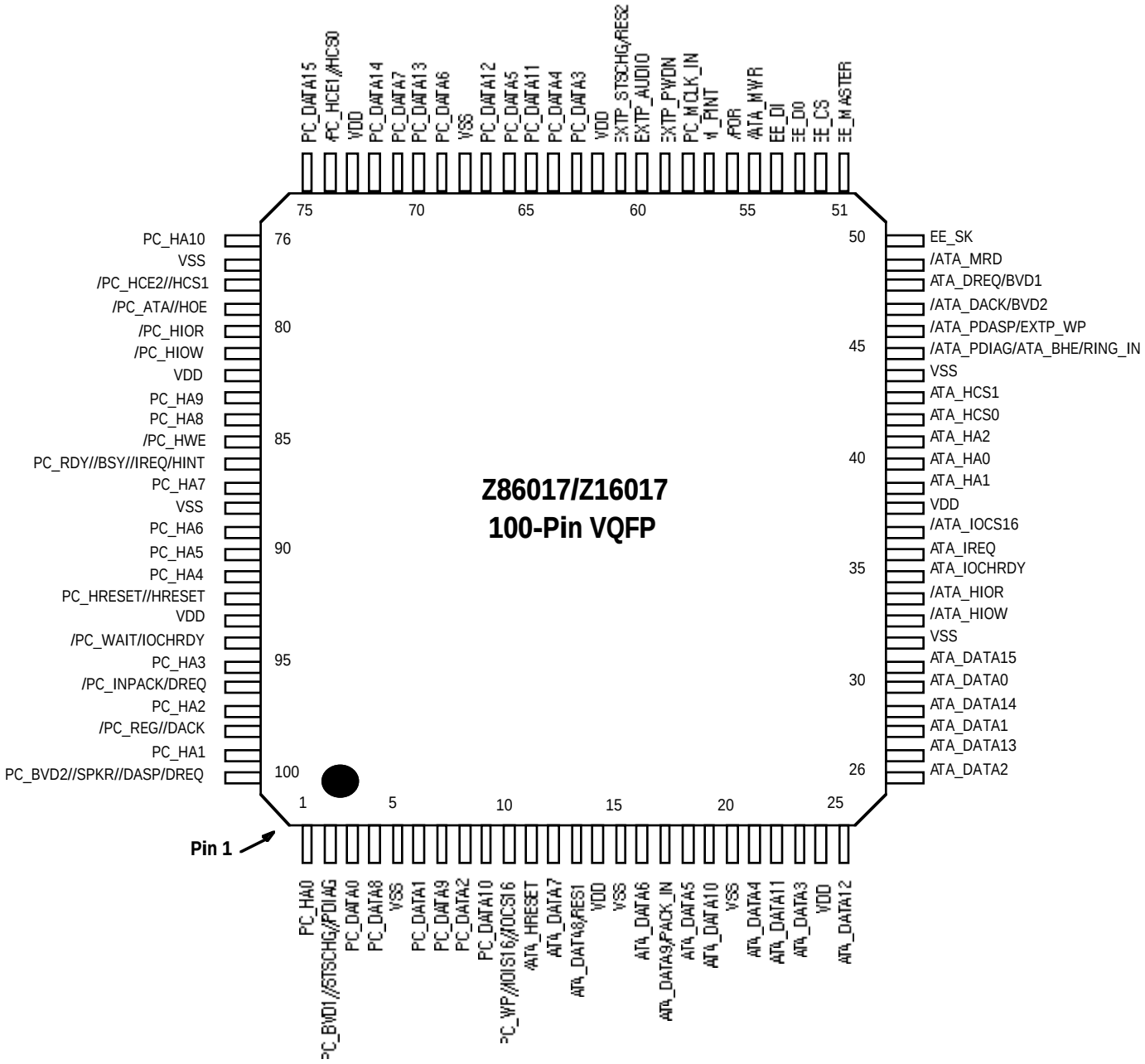

Figure 1-8. 017 100-Pin VQFP Pin Configuration

1.3 PIN DESCRIPTION (Continued)

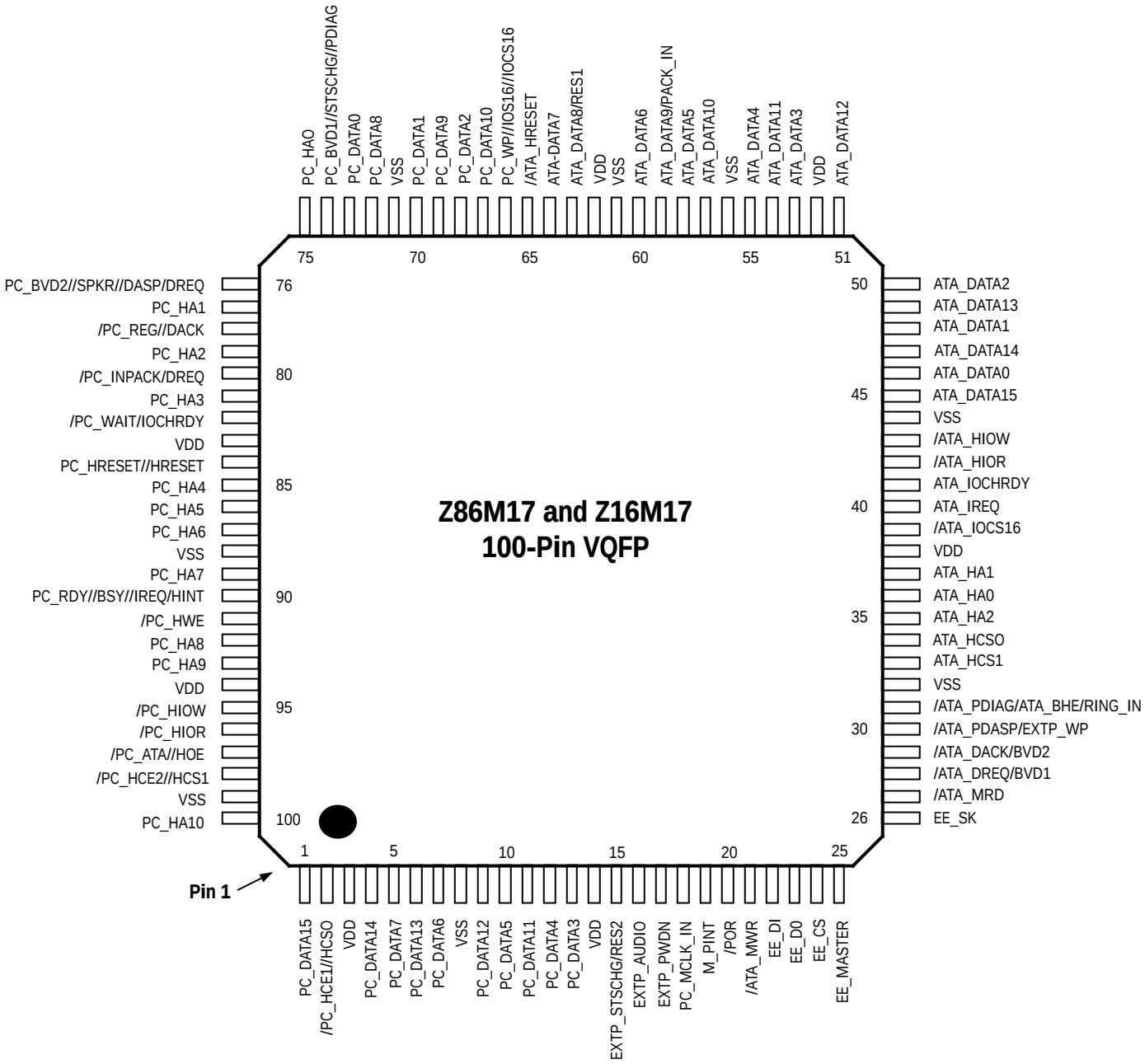

Figure 1-9. Z86M17 and Z16M17 (Mirror Image)
100-Pin VQFP Pin Configuration

1.4 PIN IDENTIFICATION

Table 1-1. 100-Pin VQFP Pin Identification

017	M17	Name	Description
1	75	PC_HA0	PCMCIA Address, Bit 0
2	74	PC_BVD1//STSCHG//PDIAG	Battery Voltage Detect 1, Status Change, PDiag
3	73	PC_DATA0	PCMCIA Data, Bit 0
4	72	PC_DATA8	PCMCIA Data, Bit 8
5	71	V_{SS}	Ground
6	70	PC_DATA1	PCMCIA Data, Bit 1
7	69	PC_DATA9	PCMCIA Data, Bit 9
8	68	PC_DATA2	PCMCIA Data, Bit 2
9	67	PC_DATA10	PCMCIA Data, Bit 10
10	66	PC_WP//IOIS16//IOCS16	Write Protect PCMCIA I/O Is 16-Bit Transfers
11	65	/ATA_HRESET	AT Host RESET
12	64	ATA_DATA7	AT Host Data, Bit 7
13	63	ATA_DATA8/RES1	AT Host Data, Bit 8, Reserved Input 1
14	62	V_{DD}	Supply Voltage
15	61	V_{SS}	Ground
16	60	ATA_DATA6	AT Host Data, Bit 6
17	59	ATA_DATA9/PACK_IN	AT Host Data, Bit 9, PACK_IN
18	58	ATA_DATA5	AT Host Data, Bit 5
19	57	ATA_DATA10	AT Host Data, Bit 10
20	56	V_{SS}	Ground
21	55	ATA_DATA4	AT Host Data, Bit 4
22	54	ATA_DATA11	AT Host Data, Bit 11
23	53	ATA_DATA3	AT Host Data, Bit 3
24	52	V_{DD}	Supply Voltage
25	51	ATA_DATA12	AT Host Data, Bit 12
26	50	ATA_DATA2	AT Host Data, Bit 2
27	49	ATA_DATA13	AT Host Data, Bit 13
28	48	ATA_DATA1	AT Host Data, Bit 1
29	47	ATA_DATA14	AT Host Data, Bit 14
30	46	ATA_DATA0	AT Host Data, Bit 0
31	45	ATA_DATA15	AT Host Data, Bit 15
32	44	V_{SS}	Ground
33	43	/ATA_HIOW	AT Host I/O Write Strobe
34	42	/ATA_HIOR	AT Host I/O Read Strobe
35	41	ATA_IOCHRDY	AT Host I/O Channel Ready
36	40	ATA_IREQ	AT Host Interrupt Request
37	39	/ATA_IOCS16	AT Host I/O Is 16 Bits Wide
38	38	V_{DD}	Supply Voltage
39	37	ATA_HA1	AT Host Address, Bit 1
40	36	ATA_HA0	AT Host Address, Bit 0
41	35	ATA_HA2	AT Host Address, Bit 2
42	34	ATA_HCS0	AT Host Chip Select 0
43	33	ATA_HCS1	AT Host Chip Select 1
44	32	V_{SS}	Ground

1.4 PIN IDENTIFICATION (Continued)

Table 1-1. 100-Pin VQFP Pin Identification

017	M17	Name	Description
45	31	/ATA_PDIAG/ATA_BHE/Ring_IN	PDIAG I/O, Byte High Enable, RING_IN
46	30	/ATA_PDASP/EXTP_WP	PDASP I/O or Write Protect In
47	29	/ATA_DACK/BVD2	AT Host DMA Acknowledge, Battery Voltage Input 2
48	28	ATA_DREQ/BVD1	AT Host DMA Request, Battery Voltage Input 1
49	27	/ATA_MRD	AT Host Memory Read Strobe
50	26	EE_SK	EEPROM Data Clock
51	25	EE_MASTER	EEPROM Is Master
52	24	EE_CS	EEPROM Data Chip Select
53	23	EE_DO	EEPROM Data Out
54	22	EE_DI	EEPROM Data In
55	21	/ATA_MWR	AT Host Memory Write Strobe
56	20	/POR	Power-On Reset
57	19	M_PINT	Local Processor Interrupt
58	18	PC_MCLK_IN	Master Clock In
59	17	EXTP_PWDN	Power Down Output
60	16	EXTP_AUDIO	Audio Input
61	15	EXTP_STSCHG/RES2	Status Change Input, Reserved Input 2
62	14	V_{DD}	Supply Voltage
63	13	PC_DATA3	PCMCIA Data, Bit 3
64	12	PC_DATA4	PCMCIA Data, Bit 4
65	11	PC_DATA11	PCMCIA Data, Bit 11
66	10	PC_DATA5	PCMCIA Data, Bit 5
67	9	PC_DATA12	PCMCIA Data, Bit 12
68	8	V_{SS}	Ground
69	7	PC_DATA6	PCMCIA Data, Bit 6
70	6	PC_DATA13	PCMCIA Data, Bit 13
71	5	PC_DATA7	PCMCIA Data, Bit 7
72	4	PC_DATA14	PCMCIA Data, Bit 14
73	3	V_{DD}	Supply Voltage
74	2	/PC_HCE1//HCS0	PCMCIA Card Enable 1 /ATA Chip Select 0
75	1	PC_DATA15	PCMCIA Data, Bit 15
76	100	PC_HA10	PCMCIA Address, Bit 10
77	99	V_{SS}	Ground
78	98	/PC_HCE2//HCS1	PCMCIA Card Enable 2 /ATA Chip Select 1
79	97	/PC_ATA//HOE	Mode Select /PCMCIA Output Enable
80	96	/PC_HIOR	PCMCIA I/O Read Strobe
81	95	/PC_HIOW	PCMCIA I/O Write Strobe
82	94	V_{DD}	Supply Voltage
83	93	PC_HA9	PCMCIA Address, Bit 9
84	92	PC_HA8	PCMCIA Address, Bit 8
85	91	/PC_HWE	PCMCIA Write Enable
86	90	PC_RDY//BSY//IREQ/HINT	PCMCIA Ready/Busy, Interrupt Request
87	89	PC_HA7	PCMCIA Address, Bit 7

Table 1-1. 100-Pin VQFP Pin Identification

017	M17	Name	Description
88	88	V_{SS}	Ground
89	87	PC_HA6	PCMCIA Address, Bit 6
90	86	PC_HA5	PCMCIA Address, Bit 5
91	85	PC_HA4	PCMCIA Address, Bit 4
92	84	PC_HRESET//HRESET	PCMCIA Reset
93	83	V_{DD}	Supply Voltage
94	82	/PC_WAIT/IOCHRDY	PCMCIA Wait, /IOCHRDY
95	81	PC_HA3	PCMCIA Address, Bit 3
96	80	/PC_INPACK/DREQ	PCMCIA Input Acknowledge, DREQ
97	79	PC_HA2	PCMCIA Address, Bit 2
98	78	/PC_REG//DACK	PCMCIA Register Signal, DACK
99	77	PC_HA1	PCMCIA Address, Bit 1
100	76	/PC_BVD2//SPKR//DASP/DREQ	PCMCIA Battery Voltage Detect 2, Speaker Output, DASP, DREQ

1.5 PIN FUNCTIONS

1.5.1 PCMCIA Signals

PC_DATA<15:0> *(I/O, Tri-State, 8 mA)*

PCMCIA Mode: 16-bit host Data bus.

ATA/IDE Mode: 16-bit host Data bus.

PC_HA<10:3> *(Input)*

PCMCIA Mode: Host Address lines: 10,9,8,7,6,5,4,3.

ATA/IDE Mode: Not used.

PC_HA<2:0> *I(nput)*

PCMCIA Mode: Host Address lines: 2,1,0.

ATA/IDE Mode: Host Address lines: 2,1,0.

/PC_HCE1//HCS0 *(Input, 100K Pull-Up)*

PCMCIA Mode: This signal is Card Enable 1 (active Low).

ATA/IDE Mode: Host Chip Select 0 (active Low).

/PC_HCE2//HCS1 *(Input, 100K Pull-Up)*

PCMCIA Mode: This signal is Card Enable 2 (active Low).

ATA/IDE Mode: Host Chip Select 1 (active Low).

/PC_REG//DACK *(Input, 100K Pull-Up)*

PCMCIA Mode: (/REG), Register bit is asserted when the host selects I/O or Attribute Memory.

ATA/IDE Mode: Data acknowledge (/DACK) defined in ATA. Issued during DMA data transfers on the data bus.

/PC_ATA//HOE *(Input, 100K Pull-Up)*

PCMCIA Mode: Memory Output Enable Strobe.

ATA/IDE Mode: When pulled Low on Power-On Reset, this signal indicates ATA/IDE mode.

/PC_HWE *(Input, 100K Pull-Up)*

PCMCIA Mode: Memory Write Enable Strobe.

ATA/IDE Mode: Not used.

/PC_HIOR *(Input, 100K Pull-Up)*

PCMCIA Mode: In PCMCIA I/O mode, this is the Input/Output Read Strobe.

ATA/IDE Mode: Input/Output Read Strobe.

/PC_HIOW *(Input, 100K Pull-Up)*

PCMCIA Mode: In PCMCIA I/O mode, this is the Input/Output Write Strobe.

ATA/IDE Mode: Input/Output Write Strobe.

PC_HRESET//HRESET *(Input, Schmitt-Triggered, 100K Pull-Up)*

PCMCIA Mode: Active High input Reset signal.

ATA/IDE Mode: Active Low input Reset signal.

PC_RDY//BSY//IREQ/HINT *(Output, 8 mA)*

PCMCIA Mode: In PCMCIA memory mode, this signal is READY//BUSY. This signal will be asserted BUSY by the RESET logic. In PCMCIA I/O mode, this signal is /IREQ.

ATA/IDE Mode: When enabled, the HINT signal is used to interrupt the host (active High).

PC_WP//IOIS16//IOCS16 *(Output, Tri-State, 8 mA)*

PCMCIA Mode: In PCMCIA memory mode, this signal is Write Protected. In PCMCIA I/O mode, this signal is IOIS16 and indicates that a 16-bit capable I/O device is being accessed on the PCMCIA bus.

***ATA/IDE Mode*:** I/O chip select 16 indicates that a 16-bit transfer is active on the bus.

/PC_WAIT/IOCHRDY *(Output, Tri-State, 8 mA)*

PCMCIA Mode: Insert Wait States when held active and the chip is being selected in I/O or memory mode.

ATA/IDE Mode: Inserts Wait States when held active, and when the chip is being selected.

/PC_INPACK/DREQ *(Output, Tri-State, 8 mA)*

PCMCIA Mode: In PCMCIA I/O mode this signal is Input Acknowledge. It is asserted by the card when the card is selected and can respond to an I/O cycle at the address on the address bus.

ATA/IDE Mode: This signal is Data request (DREQ), defined in ATA. It is issued during DMA data transfers on the data bus.

PC_BVD1//STSCHG//PDIAG *(I/O, 8 mA)*

PCMCIA Memory Mode: Battery Voltage Detect 1, output.

PCMCIA I/O Mode: Status Changed. This signal is used to indicate the change of status in the Pin Replacement Register (I/O Mode) or state of the BVD1 input when in Memory Mode.

ATA/IDE Mode: Passed diagnostics.

PC_BVD2//SPKR//DASP/DREQ *(I/O, Tri-State, 10 mA)*

PCMCIA Memory Mode: Battery Voltage Detect 2, output.

PCMCIA I/O Mode: SPKR, inverted AUDIO_EXTP signal, output;

PCMCIA ATA Mode: ATA Data Request is the input pin for this signal, when DMA Enable bit is set in Window Start/Range Address registers.

ATA/IDE Mode: Drive active/Slave present DASP.

ATA_DATA<15:10> *(I/O, Tri-State, 8 mA)*

ATA/IDE Mode: Host Data Bus, bits: 15,14,13,12,11,10.

1.5.2 Peripheral or ATA/IDE Signals

ATA_DATA<15:10> *(I/O, Tri-State, 8 mA)*
ATA/IDE Mode: Host Data Bus, bits: 15,14,13,12,11,10.
Peripheral Mode: Peripheral data bus, bits: 15, 14, 13, 12, 11,10.

ATA_DATA9/PACK_IN *(I/O, Tri-State, 8 mA)*
ATA/IDE Mode: Host Data Bus, bit: 9.
Peripheral Mode: When 8-bit mode is enabled (on the Local side) ATA_DATA9 can be used as a PACK_IN input.

ATA_DATA8/RES1 *(I/O, Tri-State, 8 mA)*
ATA/IDE Mode: Host Data Bus, bit: 8.
Peripheral Mode: When 8-bit mode is enabled (on the Local side), ATA_DATA8 can be used as a RES1 input.

ATA_DATA<7:0> *(I/O, Tri-State, 8 mA)*
ATA/IDE Mode: Host Data Bus, bits: 7,6,5,4,3,2,1,0.
Peripheral Mode: Peripheral Data Bus, bits: 7,6,5,4,3,2,1,0.

ATA_HA<2:0> *(Output, 8 mA)*
ATA/IDE Mode: ATA Host Address bits used to address the IDE interface chip.
Peripheral Mode: Lower three bits offset from starting address.

/ATA_HCS0 *(Output, 8 mA)*
ATA/IDE Mode: ATA Host Chip Select 0, used to select the IDE interface chip.
Peripheral Mode: Chip Select 0 used as a chip select for an external peripheral device as defined by the address range and offset register definition.

/ATA_HCS1 *(Output, 8 mA)*
ATA/IDE Mode: ATA Host Chip Select 1, used to select the IDE interface chip.
Peripheral Mode: Chip Select 1 used as a chip select for an external peripheral device as defined by the address range and offset register definition.

/ATA_HIOR *(Output, 8 mA)*
ATA/IDE Mode: ATA Host I/O Read Strobe.
Peripheral Mode: I/O read strobe or memory read strobe, depending on configuration.

/ATA_HIOW *(Output, 8 mA)*
ATA/IDE Mode: ATA Host I/O Write Strobe.
Peripheral Mode: I/O Write Strobe or Memory Write Strobe, depending on configuration.

/ATA_IOCS16 *(Input, 100K Pull-Up)*
ATA/IDE Mode: I/O channel is 16 bits wide; input on the local ATA bus.
Peripheral Mode: I/O access is 16 bits wide.

ATA_IREQ *(Input)*
ATA/IDE Mode: ATA/IDE host Interrupt Request.
Peripheral Mode: Interrupt Request.

ATA_IOCHRDY *(Input, 100K Pull-Up)*
ATA/IDE Mode: ATA/IDE I/O Channel Ready-Input.
Peripheral Mode: I/O Channel Ready.

/ATA_HRESET *(Output, 8 mA)*
ATA/IDE Mode: ATA Host Reset-Output to the ATA/IDE controller (programmable).
Peripheral Mode: Host reset output to the peripheral device if PCMCIA signal is active (programmable).

ATA_DREQ/BVD1 *(Input)*
ATA/IDE Mode: ATA/IDE DMA request from the ATA/IDE controller.
Peripheral Mode: Peripheral bus DMA Request or when in memory mode Battery Voltage 1 Detect input.

/ATA_DACK/BVD2 *(I/O, 8 mA)*
ATA/IDE Mode: ATA/IDE host DMA Acknowledge.
Peripheral Mode: Peripheral Bus DMA Acknowledge. DMA acknowledge is generated by the 017 whenever DMA Acknowledge is enabled in the Window Start/Range Address registers and the address corresponds to the DMA address; or Battery Voltage 2 Detect input in memory mode.

/ATA_PDASP/EXTP_WP *(I/O, Tri-State, 8 mA)*
ATA/IDE Mode: ATA/IDE bus side PDASP signal controlled by internal bits ZEN_EXT_PDASP (Input) or ZEN_INT_PDASP (Output).
Peripheral Mode: When configured as a Write Protect input, this pin will disable Write on the peripheral bus side.

/ATA_PDIAG/ATA_BHE/RING_IN *(I/O, Tri-State, 8 mA)*
ATA/IDE Mode: ATA/IDE bus side PDIAG signal controlled by internal bits ZEN_EXT_PDIAG (Input) or ZEN_INT_PDIAG (Output).
Peripheral Mode: When configured as Byte High Enable for memory boards, ATA_BHE indicates High byte available, or it can be configured to be the RING_IN input signal for the I/O event indicator CCR4.

/ATA_MRD *(Output, 8 mA)*
ATA/IDE Mode: Not used.
Peripheral Mode: External Memory Read Strobe.

/ATA_MWR *(Output, 8 mA)*
ATA/IDE Mode: Not used.
Peripheral Mode: External Memory Write Strobe.

1.5.3 Serial Interface Signals

EE_DO *(Output, 8 mA, Tri-State)*

Master Mode: EEPROM data out Serial data, valid during EE_SK edge. In master mode, this signal is an output.

Slave Mode: In slave mode, this signal is an output.

EE_SK *(I/O, 8 mA)*

Master Mode: EEPROM data clock. This signal is an output in master mode. It is active during R/W cycle only.

Slave Mode: In slave mode, this signal is an input.

EE_CS *(I/O, 8 mA)*

Master Mode: EEPROM data chip select. This signal is an output in master mode.

Slave Mode: In slave mode this signal is an input. This signal is active High.

EE_DI *(Input, 100K Pull-Up)*

Master Mode: EEPROM data in. This signal is an input in master mode.

Slave Mode: In slave mode, this signal is an input.

EE_MASTER *(Input, Schmitt-Triggered, 100K Pull-Up)*

Master/Slave mode detect: When set Low, no EEPROM is present. When set High EEPROM is present.

1.5.4 Peripheral Control Signals

/POR *I(nput, Schmitt-Triggered, 100K Pull-Up*)

Local Power-On Reset signal. A 0.1µF capacitor is recommended on this pin to GND to generate a POR.

M_PINT *(Output, Tri-State, 8 mA)*

Interrupt to local microprocessor

PC_MCLK_IN *(Input, Schmitt-Triggered)*

Master Clock In. This is an input signal. This clock signal is used to generate all internal timing. All local bus signals are asynchronous to this clock.

EXTP_STSCHG/RES2 *(Input, 100K Pull-Up)*

Status Change Input. This signal outputs the value of the status changed line on the PCMCIA bus if enabled in the CCR register, or it is an input for bit 7 (RSVDEVT3) in CCR4.

EXTP_AUDIO *(Input 100K Pull-Up)*

Audio Input. This input signal reflects the audio output. This signal is active High, and the Speaker output on the PCMCIA bus is active Low.

EXTP_PWDN *(Output, 8 mA)*

Power Down Output. This signal reflects the state of the Power Down bit in the CCR.

V_{SS} *(Input)*

Ground.

V_{DD} *(Input)*

Supply Voltage.