CHAPTER 2
Z86017/Z16017 ADDRESSING MODES

2.1 INTRODUCTION

The 017 supports all PCMCIA Addressing Modes:

- PCMCIA Common Memory Mode
- PCMCIA I/O Mode
- PCMCIA ATA_IDE Mode
- Pass-through ATA/IDE-to-ATA/IDE Mode*

Note: *This mode is for users who have a 68-pin PCMCIA connector, but are using ATA/IDE protocol instead of PCMCIA protocol.

The overall 017 mode of operation is controlled by the Interface Configuration Register (00H) bits 3,2. A 00 in these two bits sets the device to ATA/IDE mode if the /PC_ATA//HOE pin is Low on power-up and into PCMCIA mode if the pin is High. Note that the default for this register is 00 and the /PC_ATA//HOE pin determines the mode of operation, PCMCIA or ATA/IDE. These addressing modes are shown in Table 2-1.

Table 2-1. 017 Addressing Modes

Mode/Bus	PCMCIA	Local Peripheral Bus	Comments
Memory	Memory	Memory	
I/O	I/O	I/O	
PCMCIA_ATA_Memory	Memory	ATA	
PCMCIA_ATA_I/O	I/O	Primary ATA Secondary ATA Contiguous ATA	Contiguous block of at least 16 I/O registers is assigned to one card.
Pass-Through Mode	ATA/IDE	ATA/IDE	

To enable the user to place the 017 into proper Addressing mode, a set of Configuration Registers and Memory Maps reside on-chip.

The four on-chip Address Maps are:

- Memory_Map_1
- Memory_Map_2
- Memory_Map_3
- PCMCIA_ATA/IDE Map

Memory_Map_1, _2 and _3 support PCMCIA Memory/IO Mode. The chip can be configured in PCMCIA Mode either by:

– Pulling the /PC_ATA/HOE pin High during RESET;

or by

– Writing 10 in Override bits (bits 3, 2) in the Interface Configuration Register 0 (address 00H), and 0 in bits 0, 1, 2, 6 of the Interface Configuration Register 02
(address 03H).

2.1 INTRODUCTION (Continued)

After the device has been placed into PCMCIA Mode, each Map can be configured independently through its set of configuration registers.

Each Memory Map contains a set of Configuration Registers consisting of:

- Window Control Register
- Window Start Address LSB Register
- Window Start/Range Address MSB
- Window Range Address LSB

The PCMCIA_ATA/IDE Map enables chip operation in PCMCIA_ATA/IDE mode. When in this mode, the chip will respond to different types of accesses, depending on the content of the following registers:

- Interface Configuration Register 02, address 03H (bits 0, 1, 6)
- Interface Configuration Register 03, address 04H (bits 0, 1, 2, 3)
- PCMCIA Exception Status Register, address 071H (bit 0)

Table 2-2. Programming PCMCIA_ATA 017 Configuration Registers

ICR_2 [1:0] addr 03	ICR_02[6] addr 03	ICR_03[3:0] addr 04	CICR_1[7:0] addr 2DH	CICR_2[7:0] addr 2EH	CCR0[5:0] addr 0AH	addr 07[0}	Description
x	x	xxxx	xxxxxxxx	xxxxxxxx	xxxxx	1	Chip will operate in ATA/IDE- to-ATA/IDE pass-through mode
11	0	xxxx	xxxxxxxx	xxxxxxxx	xxxxx	0	PCMCIA Mode
11	1	1111	FFH	FFH	00011	0	Enabled access to Primary set of IDE Task File Registers (1Fo-1F7)
11	1	1111	FFH	FFH	00011	0	Enabled access to Primary set of IDE Task File Registers (3F6-3F7)
11	1	1111	FFH	FFH	00010	0	Enabled access to Secondary set of IDE Task File Registers
11	1	1111	FFH	FFH	00001	0	PCMCIA_ATA Independent IO Mode. Chip will respond to any 1/0 access in the range 000 to 00FH
11	1	1111	FFH	FFH	00000	0	PCMCIA Independent Memory Mode. Chip will respond to any Memory access in the range 000-00FH

Tables 2-3 through 2-6 provide 017 addressing information in PCMCIA_ATA Memory and I/O Modes.

Table 2-3. PCMCIA Common Memory Mode

Function Mode	–REG	–CE2	–CE1	A0	–0E	–WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High-Z	High-Z
Byte Access	H	H	L	L	L	H	High-Z	Even-Byte
	H	H	L	H	L	H	High-Z	Odd-Byte
Word Access	H	L	L	Z	L	H	Odd-Byte	Even-Byte
Odd-Byte only access	H	L	H	X	H	L	Odd-Byte	XX

Table 2-4. PCMCIA I/O Mode

Function Mode	–REG	–CE2	–CE1	A0	–OE	–WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High-Z	High-Z
Byte Access	H	H	L	L	L	H	High-Z	Even-byte
	H	H	L	H	L	H	High-Z	Odd-byte
Word Access	H	L	L	Z	L	H	Odd-byte	Even-byte
I/O Inhibit	H	X	X	X	L	H	High-Z	High-Z
Odd-byte only access	L	L	H	X	L	H	Odd-byte	High-Z
Byte Access	L	H	L	L	H	L	X	Even-byte
	L	H	L	H	H	L	X	Odd-Byte
Word Access	L	L	L	L	H	L	Odd-byte	Even-byte
I/O Inhibit	H	X	X	X	H	L	X	X
Odd-byte only access	L	L	H	X	H	L	Odd-byte	X

Table 2-5. PCMCIA_ATA Memory Mapped Access

REG#	A10	A[9:4]	A3	A2	A1	A0	OE#	WE#
H	L	X	L	L	L	L	Read Data	Write Data
H	L	X	L	L	L	H	Error	Feature
H	L	X	L	L	H	L	Sector Count	Sector Count
H	L	X	L	L	H	H	Sector Number	Sector Number
H	L	X	L	H	L	L	Cylinder Low	Cylinder Low
H	L	X	L	H	L	H	Cylinder High	Cylinder High
H	L	X	L	H	H	L	Drive/Head	Drive/Head
H	L	X	L	H	H	H	Status	Status
H	L	X	H	L	L	L	Duplicate Even Read Data	Duplicate Even Write Data
H	L	X	H	L	L	H	Duplicate Odd Read Data	Duplicate Odd Write Data
H	L	X	H	H	L	H	Duplicate Error	Duplicate Feature
H	L	X	H	H	H	L	Alt Status	Device Control
H	L	X	H	H	H	H	Drive Address	Reserved
H	H	X	X	X	X	L	Even Read Data	Even Write Data
H	H	X	X	X	X	H	Odd Read Data	Odd Write Data

2.1 INTRODUCTION (Continued)

Table 2-6. PCMCIA_ATA I/O Mapped Access

REG#	Primary A[9:0]	Secondary A[9:0]	Contiguous A[3:0]	IORD# = L	IOWR# = L
L	1F0H	170H	00H	Read Data	Write Data
L	1F1H	171H	01H	Error	Feature
L	1F2H	172H	02H	Sector Count	Sector Count
L	1F3H	173H	03H	Sector Number	Sector Number
L	1F4H	174H	04H	Cylinder Low	Cylinder Low
L	1F5H	175H	05H	Cylinder High	Cylinder High
L	1F6H	176H	06H	Drive/Head	Drive/Head
L	1F7H	177	07H	Status	Command
L	–	–	08H	Duplicate Even Read Data	Duplicate Even Write Data
L	–	–	09H	Duplicate Odd Read Data	Duplicate Odd Write Data
L	–	–	0DH	Duplicate Error	Duplicate Feature
L	1F6H	376H	0EH	Alt Status	Device Control
L	3F7H	377H	0FH	Drive Access	Reserved