CHAPTER 3
Z86017/Z16017
PROGRAMMING INTERNAL REGISTERS

3.1 INTRODUCTION

As stated in Chapter 2, the 017 devices feature a set of on-chip programmable registers that can be programmed either by using the on-board EEPROM Sequencer (Master Mode) or by Local Microprocessor (Slave Mode). There is also a set of Card Configuration Registers which can be accessed from the PCMCIA interface. A list of the programmable registers is shown in Table 3-1.

Table 3-1. 017 Card Configuration Registers

EEPROM Address	PCMCIA Address	Register's Name	Access	POR Value	Comments
00H	NA	Interface Configuration Rg 0	R/W	00H	
01H	NA	Interrupt Enable Rg	R/W	00H	
02H	NA	Interface Configuration Rg 1	R/W	00H	
03H	NA	Interface Configuration Rg 2	R/W	00H	
04H	NA	Interface Configuration Rg 3	R/W	00H	
05H	NA	PCMCIA CCR's Base Rg	R/W	00H	
06H	NA	PCMCIA Interrupt Status Rg	R	00H	[1]
07H	NA	PCMCIA Exception Status Rg	R	00H	[1]
08H	NA	Attribute RAM Address Rg	W	XX	[1]
09H	NA	Attribute RAM Data Rg	R/W	XX	[1]
0AH	XX0H	PCMCIA Configuration Option Rg (CCR0)	R/W	00H	[6]
0BH	XX2H	PCMCIA Card Configuration and Status Rg (CCR1)	R/W	00H	[6]
0CH	XX4H	PCMCIA Pin Replacement Rg (CCR2)	R/W	00H	[6]
0DH	XX6H	PCMCIA Socket and Copy Rg (CCR3)	R/W	00H	[6]
0EH–0FH		Reserved		XX	
10H	NA	Window 1 Control Rg	R/W	01H	
11H	NA	Window 1 Start Address LSB Rg	R/W	00H	
12H	NA	Window 1 Start/Range Address MSB Rg	R/W	00H	
13H	NA	Window 1 Range Address LSB Rg	R/W	00H	
14H	NA	Window 2 Control Rg	R/W	01H	
15H	NA	Window 2 Start Address LSB Rg	R/W	00H	
16H	NA	Window 2 Start/Range Address MSB Rg	R/W	00H	
17H	NA	Window 2 Range Address LSB Rg	R/W	00H	
18H	NA	Window 3 Control Rg	R/W	01H	
19H	NA	Window 3 Start Address LSB Rg	R/W	00H	
1AH	NA	Window 3 Start/Range Address MSB Rg	R/W	00H	

3.1 INTRODUCTION (Continued)

Table 3-1. 017 Card Configuration Registers

EEPROM Address	PCMCIA Address	Register's Name	Access	POR Value	Comments
1BH	NA	Window 3 Range Address LSB Rg	R/W	00H	
1CH–1DH		Reserved		XX	
1EH	NA	EEPROM Valid Flag Byte Rg (1CH)	R/W	00H	Master Mode only
1FH	XX8H	PCMCIA I/O Event Indication Rg (CCR4)	R/W	00H	[2], [6]
20H	7F0H	EEPROM Addr/Status Rg (CCR5) Back Door	R/W	00H	[1]
21H	7F2H	EEPROM Data Rg (CCR6) Back Door	R/W	00H	[1]
22H	7F4H	EEPROM Command Rg (CCR7) Back Door	R/W	00H	[1]
23H	NA	Revision Control Rg	R/W	00H	[2]
24H	7F6H	Revision Number Rg	R		[4]
25H		Reserved	R/W	XX	
26H	NA	Bus Control Rg 1	R/W	00H	[5]
27H	NA	IOIS16 Address Control Rg	R/W	00H	[5]
28H	NA	ATA/IDE Dual Drive Control Rg	R/W	00H	[2]
29H		Reserved	R/W	00H	
2AH	NA	Power Management Timer Count Value Rg	R/W	00H	[2]
2BH	NA	Power Management Control Rg	R/W	00H	[2]
2CH	NA	Interface Configuration Rg 4	R/W	00H	[2]
2DH	NA	Configuration Index Compare Rg 1	R/W	00H	[2]
2EH	NA	Configuration Index Compare Rg 2	R/W	00H	[2]
2FH	NA	Bus Control Rg 2	R/W	00H	[2]
30H–FFH		User-Definable Attribute Memory Location 00H–CFH (208-byte)	R/W	XXH	[3]

Notes:
[1] When the 017 is in Master Mode, the user should program this location in EEPROM with 00H.
[2] User must write the Revision Number (see 017 top mark) to the Revision Control register to unlock these registers.
[3] When the 017 is in Master Mode, data at EEPROM addresses 30H–FFH will be written to locations 00H–CFH of the on-board Attribute Memory. In Slave Mode, Attribute Memory is programmed through registers 08H and 09H.
[4] The Z86017 BA Revision Number is 10H (see device top mark).
[5] These registers are only available on the Z16017.
[6] The PCMCIA base address for these registers could be set in the range of 000H–400H. At Power-On Reset (POR), the base is set to 000H.

3.2 INTERNAL REGISTERS DESCRIPTION

EEPROM Register

Address: SELECT 00H
Name: Interface Configuration Register 0
Type: Read/Write

Bit Placement	Bit Name	Description
Bits 1–0	Set Internal	Internal Clock Divider. On Power-On Reset, clock divide-by-32 selects the Master Clock. On Power-On Reset, set these bits to 0 0.Master Clock Settings are shown in Table 3-2. Bit 1 Bit 0 0 0 Slowest Clock, Clock In divide-by-32 1 1 Clock In divide-by-16 1 0 Clock In divide-by-4 1 1 Clock In
Bits 3–2	EN_OVERIDE	Overrides PCMCIA ATA mode bits, /PC_ATA//HOE selection on the PCMCIA interface. On Power-On Reset, both bits are set to 0. Sample /PC_ATA//HOE. Bit 3 Bit 2 0 0 PC_ATA//HOE Sampled to Set Mode 0 1 Forces ATA/IDE Pass Through Mode 1 0 Forces PCMCIA Mode 1 1 Reserved
Bit 4	EN_RDY_BSY	When this bit is set to 1, the PC_RDY//BSY//REQ//HINT pin is configured as RDY//BSY. To configure this pin as an IREQ/HINT, this bit should be set to 0. On Power-On Reset, the 017 automatically reads the EEPROM and also determines if a PCMCIA device is connected. After the entire attribute memory is loaded and the chip initialization is complete, the READY//BSY signal on the PCMCIA bus will indicate READY. Without an EEPROM, the device will indicate READY whenever this bit is set and the 017 has determined a PCMCIA bus is connected.
Bit 5	EN_CTR_IRQ	Enables PCMCIA Interrupt Mode. Enables ATA_IREQ pin to control PC_IREQ in I/O Mode. This bit is active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 6	EN_INT_POL	Enable local (M_PINT) processor interrupt polarity active Low. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Interrupt is active High. **Note:** M_PINT is a tri-state driven signal. Whenever an interrupt is present and enabled, M_PINT is driven. If the interrupt is programmed active High, then M_PINT is driven from tri-state to High. If the interrupt polarity selects active Low interrupts, then the interrupt is driven from tri-state to active Low. Also see Register 2CH.
Bit 7	EN_ATA_BHE	When this bit is set to 1, it enables the ATA_PDIAG/ATA_BHE/RING_IN pin to be used as a Byte High Enable pin on a local interface side. Byte High Enable is used to signify that a PCMCIA host is requesting or sending data on the high byte bus pins ATA_DATA[15-8] of the local bus. For ATA_BHE, also see Register 2FH. When set to 0, ATA_PDIAG/ATA_BHE/RING_IN is used as a local bidirectional PDIAG pin. On Power-On Reset, this bit is set to 0.

3.2 INTERNAL REGISTERS DESCRIPTION (Continued)

Table 3-2. Master Clock

Register 0 Bit 1	Register 0 Bit 0	Clock In	EEPROM CLK Timing	Interrupt Pulse* Width	Comments
0	0	50 ns	6.4 µs	204 µs	
0	1	50 ns	3.2 µs	102 µs	
1	0	50 ns	800 ns	25 µs	Recommended
1	1	50 ns	200 ns	5.25 µs	
0	0	100 ns	12.8 µs	404 µs	
0	1	100 ns	6.4 µs	204 µs	
1	0	100 ns	1.6 µs	50 µs	
1	1	100 ns	400 ns	12.5 µs	Recommended

Note: The pulse width of the /PC.IREQ signal in pulse mode is dependent on the clock period of the master clock input (TPMCKIN). The pulse width of the /PC.IREQ signal is equal to 192 x TPMCKIN.

EEPROM Register

Address: SELECT 01H

Name: Interrupt Enable Register

Type: Read/Write

Bit Placement	Bit Name	Description
Bit 0	EN_PC_INT0	Enables Local Processor interrupt when PCMCIA host has written to CCR0, the Configuration Option Register. This interrupt will stay present until this bit is set to 0. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Also see Registers 06H, 2CH.
Bit 1	EN_PC_INT1	Enables Local Processor interrupt when PCMCIA host has written to CCR1, the Card Status Register. This interrupt will stay present until this bit is set to 0. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Also see Registers 06H, 2CH.
Bit 2	EN_PC_INT2	Enables Local Processor interrupt when PCMCIA host has written to CCR2, the Pin Replacement Register. This interrupt will stay present until this bit is set to 0. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Also see Registers 06H, 2CH.
Bit 3	EN_PC_INT3	Enables Local Processor interrupt when PCMCIA host has written to CCR3, the Socket and Copy Register. This interrupt will stay present until this bit is set to 0. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Also see Registers 06H, 2CH.
Bit 4	EN_PC_INT4	Enables Local Processor interrupt when ATA_IREQ is asserted. This interrupt will stay present until this bit is set to 0. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Also see Registers 06H, 2CH.
Bit 5	EN_EXTP_WP	Enables external write protect pin as an input when set to 1. When set to 0, this bit is DASP on the local AT bus side. On Power-On Reset, this bit is set to 0. ATA_DASP is used as a DASP pin. Also see Register 02H.
Bit 6	CCR0_OVERIDE	Card Configuration Register 0 is normally written to after Power-On Reset by the PCMCIA host. If Interrupts are allowed by the local processor or EEPROM, then the PCMCIA READY/BSY signal will be configured as an interrupt signal only when the Card Configuration Register is written to. If the local processor does not want to depend on the PCMCIA host to write to CCR0, then bit CCR0_OVERIDE can be set to force the internal logic to select the PCMCIA READY/BSY as the Interrupt pin, if interrupts are enabled. This bit is active when set to 1. On Power-On Reset, set this bit to 0, no override selected. PCMCIA host must select interrupts and write to the Card Configuration Register 0.
Bit 7	EN_INPACK	Enable PCMCIA Input acknowledge when set to 1. On Power-On Reset, this bit is set to 0.

3.2 INTERNAL REGISTERS DESCRIPTION (Continued)

EEPROM Register

Address: SELECT 02H
Name: Iterface Configuration Register 1
Type: Read/Write

Bit Placement	Bit Name	Description
Bit 0	PDIAG_SET	When set to 1, this bit activates PDIAG on the PCMCIA bus side. On Power-On Reset, this bit is set to 0.
Bit 1	EN_PDIAG	When set to 1, this bit drives the PCMCIA pin on the PCMCIA side. On Power-On Reset, this bit is set to 0 (Table 3-3). Also see Registers 04H, 07H.
Bit 2	PDASP_SET	When set to 1, this bit sets the DASP pin on the PCMCIA side. On Power-On Reset, this bit is set to 0.
Bit 3	EN_DASP	When set to 1, this bit drives the DASP pin on the PCMCIA side. On Power-On Reset, this bit is set to 0 (Table 3-4).
Bit 4	EN_OR_CS01	When set to 1, this bit is active and ATA_HCS0 has the same level as ATA_HCS1. On Power-On Reset, this bit is set to 0 (Table 3-5). Also see Register 03H.
Bit 5	EN_SPKR	When set to 1, this bit is active and connects EXTP_AUDIO (inverted) to the PC_BVD2//SPKR//DASP/DREQ pin. On Power-On Reset, this bit is set to 0 (Table 3-6).
Bit 6	EN_DASP_INT	When set to 1, DASP is generated internally. On Power-On Reset, this bit is set to 0.
Bit 7	EN_DASP_EXT	When set to 1, DASP is generated externally from the AT_DASP pin on the local AT bus side. On Power-On Reset, this bit is set to 0. Also see Register 01H.

Table 3-3. PCMCIA PDIAG Pin Functions

Register2 Bit 1 EN_PDIAG	Register2 Bit 0 PDIAG_SET	Register 4 Bit 7 EN_PDIAG_EXT	Register4 Bit 6 EN_PDIAG_INT	ATA_PDIAG Pin I/O	PCMCIA PDIAGOUT I/O	Register 7 Bit5,PCMCIA PDIAG Input	Comments
0	X	X	X	X	Float - Z	PDIAG-OUT	Input mode
0	1	0	1	X	Float - Z	PDIAG-OUT	Input mode
1	1	0	1	X	1 (Output)	1	Output 1 (totem)
1	0	0	1	X	0 (Output)	0	Output 0 (totem)
1	0	1	0	0 (Input)	0 (Output)	0	Output generated from
							ATA-PDIAG.
1	0	1	0	1 (Input)	Float - Z	PDIAG-OUT	Output floated by
							ATA-PDIAG when set
							to 1.
0	0	0	1	0 (Output)	0 (Input)	0	ATA_PDIAG is sourced
							from PCMCIA side.
0	0	0	1	Float - Z	1 (Input)	1	

Table 3-4. PCMCIA DASP Pin Functions

Register2 Bit 3 EN_DASP	Register2 Bit 2 DASP_SET	Register2 Bit 7 EN_DASP_EXT	Register2 Bit 6 EN_DASP_INT	ATA_DASP Pin I/O	PCMCIA DASP OUT I/O	Register7 PCMCIA DASP Input	Comment
0	X	X	X	X	Float - Z	DASP-OUT	Input mode
0	1	0	1	X	Float- Z	DASP-OUT	Input mode
1	1	0	1	X	1 (Output)	1	Output 1 (totem)
1	0	0	1	X	0 (Output)	0	Output 0 (totem)
1	0	1	0	0 (Input)	0 (Output)	0	Output generated from ATA-DASP.
1	0	1	0	1 (Input)	Float- Z	DASP-OUT	Output floated when
							ATA-DASP is set to 1.
0	0	0	1	0 (Output)	0 (Input)	0	ATA_DASP is sourced
							from PCMCIA side.
0	0	0	1	Float - Z	1 (Input)	1	

Table 3-5. Host Chip Select Designations

Register 2 Bit 4 EN_OR_CS01	ATA_HCS0	Internal HCS1	ATA_HCS0 (External)
0	0	X	0
0	1	X	1
1	0	0	0
1	0	1	1
1	1	X	1

Table 3-6. Audio Pin Configurations

Register 2 Bit 5 EN_SPKR	EXTP_AUDIO	Register 7 Bit 0 ATA_MODE	Register 2 Bit 3 EN_DASP	PC_SPKR/ DASP//DREQ
0	X	0	0	Float - Z
1	0	0	0	1
1	1	0	0	0
1	0	0	0	AT_DREQ Input
0	0	0	0	AT_DREQ Input
0	0	1	x	DASP mode

3.2 INTERNAL REGISTERS DESCRIPTION (Continued)

EEPROM Register

Address: SELECT 03H
Name: Interface Configuration Register 2
Type: Read/Write

Bit Placement	Bit Name	Description
Bit 0	EN_MEM_MODE	Enables PCMCIA memory access mode. This bit controls window0. It is active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 1	EN_INDP_MODE	Enables PCMCIA independent I/O access mode. This bit controls window0. It is active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 2	EN_ATT_MODE	Enables PCMCIA attribute memory access. This bit is active when set to 1. On Power-On Reset, this bit is set to 0. Also see Registers 08H and 09H.
Bit 3	EN_INVERT_HCS0	Inverts the polarity of HCS0 output. HCS0 is active High when this bit is set. HCS0 is active Low when this bit is cleared. This bit is active when set to 1. On Power-On Reset, this bit is set to 0, active Low. Also see Register 02H.
Bit 4	EN_INVERT_HCS1	Inverts the polarity of HCS1 output. HCS1 is active High when this bit is set. HCS1 is active Low when this bit is cleared. This bit is active when set to 1. On Power-On Reset, this bit is set to 0, active Low. Also see Register 02H.
Bit 5	EN_INVERT_ATRST	Inverts the polarity of the ATA_HRESET output.
Bit 6	EN_IO_MODE	Enables PCMCIA/ATA/IDE access to 1Fx, 3Fx, 17x, 1Fx task Registers. This bit controls window0. This bit is active when set to 1. On Power-On-Reset, this bit is set to 0.
Bit 7	Reserved	

EEPROM Register

Address: SELECT 04H

Name: Interface Configuration Register 3

Type: Read/Write

Bit Placement	Bit Name	Description
Bit 0	SEL_PRIMARY_1x	Enables IDE/PCMCIA access to primary task file addresses 1F<0-7>. This bit is active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 1	SEL_PRINARY_3x	Enables IDE/PCMCIA access to primary task file addresses 3F<6-7>. Active when set to 1. On Power-On Reset, this bit is set to 0 (Table 3-7).
Bit 2	SEL_SECOND_1x	Enables IDE/PCMCIA access to secondary task file addresses 17<0-7>. Active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 3	SEL_SECOND_3x	Enables IDE/PCMCIA access to secondary task file addresses 37<0-7>. Active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 4	STR_RST	Switching this bit from Low to High to Low again forces the 017 to check the level on PC_ATA/HOE pin and latch the mode. This bit is active when set to 1. On Power-On Reset, this bit is set to 0.
Bit 5	EN_DIS_RST	Disable PCMCIA reset. This bit is active when set to 1. Resets from the PCMCIA bus are not allowed. On Power-On Reset, this bit is set to 0 (Table 3-8).
Bit 6	EN_PDIAG_INT	When this bit is set to 1, PDIAG is generated internally. On Power-On Reset, this bit is set to 0. Also see Registers 02H and 07H.
Bit 7	EN_PDIAG_EXT	When this bit is set to 1, PDIAG is generated externally through the AT_PDIAG pin on the local AT side. On Power-On Reset, this bit is set to 0. Also see Registers 02H and 07H.

Table 3-7. ATA Register Selection Designations

Register 4 Bit 3 SEL_SECOND_3x	Register 4 Bit 2 SEL_SECOND_1x	Register 4 Bit 1 SEL_PRIMARY_3x	Register 4 Bit 0 SEL_PRIMARY_1x	Register 3 Bit 6 EN_IO_MODE	Address Range Response	Note
X	X	X	X	0	XX	Disabled
0	0	0	0	1	XX	Disabled
0	0	0	1	1	1F0-1F7	Primary HDD
0	0	1	1	1	1F0-1F7,3F6,3F7	Primary HDD
0	1	0	0	1	170-177	Secondary HDD
1	1	0	0	1	170-177,376,377	Two drive system on local
1	1	1	1		170-177,376,377,1F0-1F7 3F6,3F7	AT bus side

3.2 INTERNAL REGISTERS DESCRIPTION (Continued)

Table 3-8. Reset Conditions

Register 4 Bit 5 EN_DIS_RST	PC_HRESET	Register 7 Bit 0 ATA_MODE	ATA_HRESET	Notes:
1	X	X	1	PCMCIA Mode, Reset Disabled
0	0	0	1	PCMCIA Mode, No Reset
0	1	0	0	PCMCIA Mode, Asserted Reset
0	1	1	1	ATA Mode, No Reset.
0	0	1	0	ATA Mode, Asserted Reset.

EEPROM Register

Address: SELECT 05H
Name: BCMCIA CCR Base Address
Type: Read/Write

Bit Placement	Bit Name	Description
Bit 0	EN_CRR_A4	Enables address bit 4 to be compared as High on PCMCIA when the PCMCIA Configuration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 1	EN_CRR_A5	Enables address bit 5 to be compared as High on PCMCIA when the PCMCIA Configuration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 2	EN_CRR_A6	Enables address bit 6 to be compared as High on PCMCIA when the PCMCIA Configuration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 3	EN_CRR_A7	Enables address bit 7 to be compared as High on PCMCIA when the PCMCIA Configuration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 4	EN_CRR_A8	Enables address bit 8 to be compared as High on PCMCIA when the PCMCIA Configuration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 5	EN_CRR_A9	Enables address bit 9 to be compared as High on PCMCIA when the PCMCIA Configuration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 6	EN_CRR_A10	Enables address bit 10 to be compared as High on PCMCIA when the PCMCIA Configuration Register's base address is accessed. On Power-On Reset, this bit is set to 0.
Bit 7	DIS_CRR_MODE	Disables PCMCIA host and allows access to the PCMCIA Configuration Register's base address. This bit is active when set to 1. On Power-On Reset, this bit is set to 0.

Table 3-9. CCR Location Examples

Register5 Bit 7 EN	Register5 Bit 6 A10	Register5 Bit 5 A9	Register5 Bit 4 A8	Register5 Bit 3 A7	Register5 Bit 2 A6	Register5 Bit 1 A5	Register5 Bit 0 A4	CCR Base Address
1	X	X	X	X	X	X	X	None
0	0	0	0	0	0	0	0	0000Hx
0	0	0	0	0	0	0	1	0010Hx
0	0	1	0	0	0	0	0	0200Hx
0	1	0	0	0	0	0	0	0400Hx

EEPROM Register

Address: SELECT 06H

Name: PCMCIA Interrupt Status Register

Type: Read

Bit Placement	Bit Name	Description
Bit 0	PC_INT0	PCMCIA host write to CCR0, the Configuration Option Register has occurred. This bit is active when set to 1. Also see Register 01H.
Bit 1	PC_INT1	PCMCIA host write to CCR1, the Card Configuration and Status Register has occurred. This bit is active when set to 1. Also see Register 01H.
Bit 2	PC_INT2	PCMCIA host write to CCR2, the Pin Replacement Register has occurred. This bit is active when set to 1. Also see Register 01H.
Bit 3	PC_INT3	PCMCIA host write to CCR3, the Socket and Copy Register has occurred. This bit is active when set to 1. Also see Register 01H.
Bit 4	PC_INT4	External ATA_IREQ interrupt has occurred. This bit is active when set to 1. Also see Register 01H.
Bit 5	PC_INT5	PCMCIA host write to CCR4, an I/O Event Indication Register has occurred. This bit is active when set to 1.
Bit 6	REV_BA	Set this bit to 1 after writing the revision number (see device top mark) to the revision control Register.
Bit 7	Reserved	

3.2 INTERNAL REGISTERS DESCRIPTION (Continued)

EEPROM Register

Address: SELECT 07H
Name: PCMCIA Exception Status Register
Type: Read

Bit Placement	Bit Name	Description
Bit 0	ATA/IDE_MODE	When bit 7 of this register is set to 1, ATA mode has been selected by sampling the /PC_ATA//HOE signal on Power-On-Reset, or the override bits in Register 0 have set the 017 to run in ATA/IDE mode. When set to 0, this bit indicates that the 017 will operate in PCMCIA mode (Table 3-10).
Bit 1	PCRST	PCMCIA reset status. Active when set to 1.
Bit 2	Reserved	
Bit 3	Reserved	
Bit 4	Reserved	
Bit 5	PDIAG	PDIAG is present. This bit is active when set to 1.
Bit 6	DASP	DASP is present. Drive Active/Slave Present. This bit is active when set
Bit 7	ATA_SAMPLED	When set to 1, this bit indicates that bit 0 of this register is valid to read.

Table 3-10. ATA Sample Mode Bit

Register 7 Bit 7 ATA_SAMPLED	Register 7 Bit 0 ATA_MODE	Comments
0	X	Not ready
1	0	PCMCIA Addressing Mode
1	1	ATA/IDE Addressing Mode

EEPROM Register

Address: SELECT 08H
Name: Attribute Memory Address
Type: Write

Bit Placement	Bit Name	Description
Bits 7-0	Attribute Memory Address	After each access to the attribute RAM data register, the address is automatically incremented. Also see Register 03H.

EEPROM Register

Address: SELECT 09H
Name: Attribute Memory Data
Type: Write/Read

Bit Placement	Bit Name	Description
Bits 7-0	Attribute Memory Data	The data read and written from this register is associated with the attribute memory location pointed to by the attribute RAM data address register. After each data write or read into this location, the address is automatically incremented by one. Also see Register 03H.

EEPROM Register

Address: SELECT 10H
Name: Window 1 Control Register
Type: Write/Read

Bit Placement	Bit Name	Description
Bit 0	DIS_PAC1	When this bit is set to 1, the Port 1 Address Control and decoder are disabled.
Bit 1	EN_PAC1_MEM	When this bit is set to 1, Memory Mode decoder is enabled. When cleared, I/O mode is enabled.
Bit 2	EN_PAC1_16	When this bit is set, data swapping is provided internal to the chip during data reads from the low byte of the ATA bus to the PCMCIA bus high byte, and from the high byte of the PCMCIA bus to the low byte of the ATA bus during data writes. When cleared, it is high byte to high byte and low byte to low byte.
Bit 3	READ_PROTECT	Allows two cards at the same address to be read. When this bit is set, it prevents the PCMCIA bus from becoming active.
Bit 4	EN_PAC1_ADDR_COMP	When this bit is set, use address compare logic, when it is cleared, acknowledge all PCMCIA chip selects.
Bit 5	EN_PAC1_HCS	When this bit is set, HCS1 is used as an external chip select, when it is cleared, HCS0 is used as an external chip select. Also see Registers 02H and 03H.
Bits 7-6		Number of wait states (in Master Clock periods) inserted on the PCMCIA bus. 00 = 0xTpmckin (no wait states) 01 = 4x Tpmckin 10 = 5x Tpmckin 11 = 7x Tpmckin

3.2 INTERNAL REGISTERS DESCRIPTION (Continued)

EEPROM Register

Address: SELECT 11H
Name: Window 1 Start Address LSB
Type: Write/Read

Bit Placement	Bit Name	Description
Bits 7-0		LSB starting address for Port 1.

EEPROM Register

Address: SELECT 12H
Name: Window 1 Start/Range Address MSB
Type: Write/Read

Bit Placement	Bit Name	Description
Bits 2-0		Bits 8, 9, and 10 of the starting address range of Port 1.
Bit 3	EN_WRITE_PROTECT	When this bit is set, the RWPROT bit in the pin replacement register is used to inhibit writing to the external peripherals. When these bits are cleared, PROT is ignored.
Bits 6-4		Bits 8, 9, and 10 of the starting address range of Port 1.
Bit 7	EN_DMA_ACK	When this bit is set, ATA_DMA_ACKNOWLEDGE is set when the address space is accessed, and Speaker Out on the PCMCIA interface is used as DREQ.

EEPROM Register

Address: SELECT 13H
Name: Window 1 Range Address LSB
Type: Write/Read

Bit Placement	Bit Name	Description
Bits 7-0		LSB range Address for Port 1

EEPROM Register

Address: SELECT 14H
Name: Window 2 Control Register
Type: Write/Read

Bit Placement	Bit Name	Description
Bit 0	DIS_PAC2	When this bit is set to 1, it disables Port 2 address control and decoder.
Bit 1	EN_PAC2_MEM	When this bit is set to 1, Memory Mode decoder is enabled. When it is cleared, the I/O Mode decoder is enabled.
Bit 2	EN_PAC2_16	When this bit is set, data swapping is provided internal to the chip during data reads from the low byte of the ATA bus to the PCMCIA bus high byte, and from the high byte of the PCMCIA bus to the low byte of the ATA bus during data writes. When this bit is cleared, it is high byte to high byte and low byte to low byte.
Bit 3	READ_PROTECT	Allows two cards at the same address to be read from. When this bit is set, it will prevent the PCMCIA bus from becoming active.
Bit 4	EN_PAC2_ADDR_COMP	When this bit is set, use address compare logic, when it is cleared, acknowledge all PCMCIA chip selects.
Bit 5	EN_PAC2_HCS	When this bit is set, HCS1 is used as an external chip select, when it is cleared, HCS0 is used as an external chip select. Also see Registers 02H and 03H.
Bits 7-6		Number of wait states (in Master Clock period) inserted on the

EEPROM Register

Address: SELECT 15H
Name: Window 2 Start Address LSB
Type: Write/Read

Bit Placement	Bit Name	Description
Bits 7-0		LSB starting address for Port 2.

3.2 INTERNAL REGISTERS DESCRIPTION (Continued)

EEPROM Register

Address: SELECT 16H
Name: Window 2 Start/Range Address MSB
Type: Write/Read

Bit Placement	Bit Name	Description
Bits 2-0		Bits 8, 9, and 10 of the starting address range of Port 2.
Bit 3	EN_WRITE_PROTECT	When this bit is set, the RWPROT bit in the pin replacement register is used to inhibit writing to the external peripherals. When it is cleared, PROT is ignored.
Bits 6-4		Bits 8, 9, and 10 of the starting address range of Port 2.
Bit 7	EN_DMA_ACK	When this bit is set, ATA_DMA_ACKNOWLEDGE is set when the address space is accessed, and Speaker Out on the PCMCIA interface is used as DREQ.

EEPROM Register

Address: SELECT 17H
Name: Window 2 Range Address LSB
Type: Write/Read

Bit Placement	Bit Name	Description
Bits 7-0		LSB range address for Port 2.

EEPROM Register

Address: SELECT 18H
Name: Window 3 Control Register
Type: Write/Read

Bit Placement	Bit Name	Description
Bit 0	DIS_PAC3	When set to 1, this bit disables Port 3 address control and decoder.
Bit 1	EN_PAC3_MEM	When this bit is set to 1, Memory mode decoder is enabled. When it is cleared, I/O mode decoder is enabled.
Bit 2	EN_PAC3_16+	When this bit is set, data swapping is provided internal to the chip during data reads from the low byte of the ATA bus to the PCMCIA bus high byte, and from the high byte of the PCMCIA bus to the low byte of the ATA bus during data writes. When this bit is cleared, it is high byte to high byte and low byte to low byte.
Bit 3	READ_PROTECT	This bit allows two cards to be read from the same address. When this bit is set, it will prevent the PCMCIA bus from becoming active.
Bit 4	EN_PAC3_ADDR_COMP	When this bit is set, use address compare logic, when it is cleared, acknowledge all PCMCIA chip selects.
Bit 5	EN_PAC3_HCS	When this bit is set, HCS1 is used as an external chip select, when it is cleared, HCS0 is used as an external chip select.
Bits 7-6		Number of wait states (in Master Clock periods) inserted on the PCMCIA bus.

EEPROM Register

Address: SELECT 19H
Name: Window 3 Start Address LSB
Type: Write/Read

Bit Placement	Bit Name	Description
Bits 7-0		LSB starting Address for Port 3.

3.2 INTERNAL REGISTERS DESCRIPTION (Continued)

EEPROM Register

Address: SELECT 1AH
Name: Window 3 Start/Range Address MSB
Type: Write/Read

Bit Placement	Bit Name	Description
Bits 2-0		Bits 8, 9, and 10 of the starting address range of Port 3.
Bit 3	EN_WRITE_PROTECT	When this bit is set, the RWPROT bit in the pin replacement register is used to inhibit writing to the external peripherals. When this bit is cleared, PROT is ignored.
Bits 6-4		Bits 8, 9, and 10 of the starting address range of Port 3.
Bit 7	EN_DMA_ACK	When this bit is set, ATA_DMA_Acknowledge is set when the address space is accessed, and Speaker Out on the PCMCIA interface is used as DREQ.

EEPROM Register

Address: SELECT 1BH
Name: Window 3 Range Address LSB
Type: Write/Read

Bit Placement	Bit Name	Description
Bits 7-0		LSB range address for Port 3.

EEPROM Register

Address: SELECT 1EH
Name: EEPROM Valid Flag Byte
Type: Read

Bit Placement	Bit Name	Description
Bits 7-0	Flag Byte	Read-Only Register used by the internal EEPROM Sequencer to Determine if the contents of the EEPROM are valid. The valid Flag value is 1CH.

EEPROM Register

Address: SELECT 20H
Name: EEPROM ADDR/STATUS CCR5 Back Door
Type: Write/Read

Bit Placement	Bit Name	Description
Bits 7-0	Address/Status Bits	EEPROM address/status data.

EEPROM Register

Address: SELECT 21H
Name: EEPROM DATA CCR6 Back Door
Type: Write/Read

Bit Placement	Bit Name	Description
Bits 7-0	Data Bits	EEPROM data.

EEPROM Register

Address: SELECT 22H
Name: EEPROM Command CCR7 Back Door
Type: Write/Read

Bit Placement	Bit Name	Description
Bits 7-0	Command Bits	Command value.

3.2 INTERNAL REGISTERS DESCRIPTION (Continued)

EEPROM Register

Address: SELECT 23H
Name: Revision Control Register
Type: Read/Write

Bit Placement	Bit Name	Description
Bit 3-0	REV_MINOR	The lower four bits determine the minor revision number. This nibble must be written with the value read back from the lower nibble in Read-Only Register 24H to enable the minor revision functions.
Bit 7-4	REV_MAJOR	The upper four bits determine the major revision number. This nibble must be written with the value read back from the upper nibble in Read-Only Register 24H to enable the major revision functions.

EEPROM Register

Address: SELECT 24H
Name: Revision Number Register
Type: Read

Bit Placement	Bit Name	Description
Bit 3-0	REV_NUM_MINOR	This is the Read-Only minor revision number of the chip.
Bit 7-4	REV_NUM_MAJOR	This is the Read-Only major revision number of the chip.

Note: Registers 26H and 27H are only available on the Z16017 device.

EEPROM Register

Address: SELECT 26H
Name: :Bus control 1
Type: Read/Write
Reset: 00h

Bit Placement	Bit Name	Description
Bit 0	DISABLE_CLK	When this bit is set to 1, it turns off the PC_MCLK_IN pad. When it is cleared, it enables the PC_MCLK_IN pad. This bit is automatically cleared when in Master mode and at any access to the EEPROM command Register 7F4H as seen through the PCMCIA interface.
Bit 1	EN_IOIS_IN	When this bit is set to 1, it enables the IOIS16 signal to be generated internally (see Register 27, IOIS16 Address Control Register). When it is cleared, the source for IOIS16 will be the ATA_IOIS16 input.
Bit 3-2	8-Bit_CNTRL	PCMCIA 8- to 16-bit control enable (see Table 3.12).
Bit 4	EN_RW_LONG	Set this bit to 1 to enable the read/write long function when using the 8-bit to 16-bit mode or internal IOCS16 generation in ATA/IDE pass-through mode. **PCMICA 8-Bit to 16-Bit Access** After 512 bytes are transferred, each PC_IOR/IOW strobe to the data register will generate a ATA_IOR/IOW strobe on the ATA/IDE bus. 8-bit to 16-bit accesses of the data register will be continued after any write access to a task file register other than the data register. **ATA/IDE Pass Through Mode** When set in ATA/IDE pass-through mode after 256 word accesses of the data register, the //IOCS16 signal on the host interface will de-assert until the next data transfer phase. The internal IOCS16 function must also be enabled. (EN_IOIS_IN=1) and the IOIS16 ADDR register set to 01 pointing to the ATA/IDE task file data Register 1F0, 170. Clearing this bit will disable the read/write long function.
Bit 6-5	IOIS16_CTRL	IOIS16 source select (see Table 3.11)
Bit 7	BVD_CTRL	When set to 1, this bit enables the PC_BVD1//STSCHG//PDIAG and PC_BVD2//SPKR//DASP//DREQ functions. When cleared, it sets both PC_BVD1/ /STSCHG//PDIAG and PC_BVD2//SPKR//DASP /DREQ pins High when in PCMCIA ATA/IDE memory mode. At Power-On Reset, set to 0.

3.2 INTERNAL REGISTERS DESCRIPTION (Continued)

Note: Registers 26H and 27H are only available on the Z16017 device.

EEPROM Register

Address: SELECT 27H
Name: IOIS16 Address Control
Type: Read/Write
Reset: 00h

The contents of this register determine which on-Host address IOIS16 should be generated, but only when bit 1 of Register 26H is set to 1.

Register Content Bit <7-0>	Host Address PC_HA <3-0>	PC_WP//IOIS16//IOIS16	Comments
10000000 (80H)	1110 (EH)	0	Must use this address to generate IOIS16.*
01000000 (40H)	1100 (CH)	0	
00100000 (20H)	1010 (AH)	0	
00010000 (10H)	1000 (8H)	0	
00001000 (08H)	0110 (6H)	0	
00000100 (04H)	0100 (4H)	0	
00000010 (02H)	0010 (2H)	0	
00000001 (01H)	0000 (0H)	0	

Note: * In order for IOIS16 to be generated on any even address, the register should contain 1 in all positions.

Table 3-11. IOIS16_CTRL

Bit 6	Bit 5	Description
0	0	/IOIS16 is being generated internally.
0	1	
1	0	IOIS8 is the source for the IOIS16 in PCMCIA I/O Mode.
1	1	IOIS16 is always High in PCMCIA I/O Mode

Note: IOIS8 is bit 5 in CCR1 Card Configuration and Status Register.

Table 3-12. 8-bit _CTRL

Bit 3	Bit 2	Description
0	0	PCMCIA_8 to ATA_16 Mode is disabled.
0	1	
1	0	IOIS8 controls PCMCIA_8 to ATA_16 Mode.
1	1	Forces the 017 into PCMCIA_8 to ATA_16 Mode.

Note: IOIS8 is bit 5 in CCR1 Card Configuration and Status Register.

EEPROM Register

Address: SELECT 28H
Name: ATA/IDE Dual Drive Control
Type: Read/Write

Bit Placement	Bit Name	Description
Bit 0	M_S_enable	This bit enables the Master/Slave mode control. When this bit is set to 1, the Master/Slave function is enabled. When it is set to 0, this function is disabled.
Bit 1	Drive_select	When programmed, this bit determines when to drive the ATA/IDE bus. When set to 1, the 017 will drive the ATA bus when the host writes a 1 into Bit 4 of the “Drive/Head” task file register. Both primary and secondary addresses are compared. If this bit is set to 0, then the 017 drives the bus if the host writes a 0 into Bit 4 of the “Drive/Head” task file register.
Bit 7-2	Reserved	Unused

Note: Read Back Values: Z86017 00010000b = 10H
Z16017 00100000b = 20H

EEPROM Register

Address: :SELECT 2AH
Name: Power Management Timer Count Value
Type: :Read/Write

Bit Placement	Bit Name	Description
Bit 7-0	TIMER_VAL	Power management timer count value. The timer will be reset during all PCMCIA activity. When the timer expires, it will power-down all noncritical signals. TIMER intervals (sec.) = PC_MCLK (sec.) * 2(27) * timer_val. For example: PC_MCLK (20 MHz, 50 ns) *2(27) * 1 = 6.67 sec. Also see Register 2CH.

3.2 INTERNAL REGISTERS DESCRIPTION (Continued)

EEPROM Register

Address: SELECT 2BH

Name: Power Management Control Register

Type: Read/Write

Bit Placement	Bit Name	Description
Bit 0	EN_8BIT_MODE	When set to 1, this bit enables the 8-bit mode on the local interface. When cleared, it enables the 16-bit interface.
Bit 1	EN_MODEM_ALT	When set to 1, this bit enables the alternate modem functions/pins. When cleared, it disables modem functions.
Bit 2	EN_CLK	When this bit is set to 1, all internal clocks are disabled after loading from the serial EEPROM. When this bit is cleared, all clocks are enabled.
Bit 3	EN_PADS	When this bit is set to 1, the PCMCIA external pads are powered-down, unless PCMCIA* PC_HCE1 and PC_HCE2 are active. When this bit is cleared, all external pads are enabled.
Bit 4	EN_TIMER	When this bit is set to 1, the power management timer is enabled. The timer value is contained in Register 2A. When this bit is cleared, the power management timer is held reset and disabled.
Bit 5	EN_PM_RDY	When this bit is set to 1, the 017 will set BUSY on the PCMCIA interface when the host sets the power-down bit in CCR1.
Bit 6	EN_EXT_PD	When this bit is set to 1, the power management timer will activate the external power-down signal EXTP_PWND. When this bit is cleared, the external signal will not be activated. Also see Register 0BH.
Bit 7	EN_EXPD_POL	When this bit is set to 1, the external power-down signal EXTP_PWND is active Low. When this bit is cleared, EXTP_PWND is active High.

Note: *When the “En_Pads” bit is set, access to the CCR Registers is disabled.

EEPROM Register

Address: SELECT 2CH

Name: Interface Configuration Register 4

Type: Read/Write

Bit Placement	Bit Name	Description
Bit 2-0	TSTCLK	These power management clock select bits can be used to provide delay times in a number of different scales. Table 3-13 shows the different delay scale settings. Also see Register 2AH.
Bit 3	EN_POLL_BSY	This bit allows the 017 to poll the Busy status bit in the local controller task file. When enabled in PCMCIA ATA I/O mode, the Busy status bit in the local controllers task file is latched into the pin replacement register. In PCMCIA ATA Memory mode, the Busy status bit is put on the Ready/Busy signal. Set this bit to 1 to enable auto polling. When this bit is cleared, auto polling is disabled. On Power-On Reset, it is set to 0.
Bit 4	EN_GLOB_INT	This is a Global Interrupt Enable for the M-PINT pin. When set to 1, this bit enables the local µP interrupts. When cleared, it disables the local µP interrupt. On Power-On Reset, it is set to 0.
Bit 5	EN_PC_INT5	This bit enables the local Processor interrupt when the PCMCIA host has written to the I/O event indication Register CCR4. This interrupt source stays present until this bit is set to 0. When set to 1, this bit is active. On Power-On Reset, it is set to 0.
Bit 6	EN_BVD_INPUTS	When set to 1, this bit enables the two BVD inputs to be reflected either in Pin Replacement Register or on the corresponding pins of the 017. On Power-On Reset, it is set to 0. (Also see register 0CH.)
Bit 7	EN_PULSE	When set, this bit enables auto busy status when the host sets reset. The busy status remains present until the internal time-out or when using a µP and the µP clears the busy status. When cleared, this bit disables auto busy on host resets. The pulse time for busy is 2^{15}/PC_MCLK (MHz) = SEL.

Table 3-13. Power Management Clock Select

Bit 2 0	Bit 1 0	Bit 0 0	Timer/Count 6.7 sec./count	Input Clock PC_MCLK @ 20 MHz
0	0	1	6.4 µsec./count	@ 20 MHz
0	1	0	Disable counter	
0	1	1	12.8 µsec./count	@ 20 MHz
1	0	0	100 nsec./count	@ 20 MHz
1	0	1	6.4 µsec./count	@ 20 MHz
1	1	0	6.4 µsec./count	@ 20 MHz

3.2 INTERNAL REGISTERS DESCRIPTION (Continued)

EEPROM Register

Address: SELECT 2DH
Name: Configuration Index Compare Register 1
Type: Read/Write

Bit Placement	Bit Name	Description
Bit 2-0	IO_SEL_SEC	These bits are the configuration index for I/O secondary select.
Bit 3	EN_ IO_SEL_SEC	When set to 1, this bit enables the configuration index I/O secondary select; when cleared, it is disabled.
Bit 6-4	IO_SEL_PRI	These bits are the configuration index for I/O primary select.
Bit 7	EN_IO_SEL_PRI	When set to 1, this bit enables the configuration index I/O primary select; when cleared, it is disabled.

EEPROM Register

Address: :SELECT 2EH
Name: Configuration Index Compare Register 2
Type: Read/Write

Bit Placement	Bit Name	Description
Bit 2-0	MEM_INDX	These bits are the configuration index for memory select.
Bit 3	EN_MEM_INDX	When set to 1, this bit enables configuration index memory select; when cleared, it is disabled.
Bit 6-4	IO_INDP_INDX	These bits are the configuration index for I/O independent select.
Bit 7	EN_IO_INDP_INDX	When set to 1, this bit enables configuration index independent select; when cleared, it is disabled.

EN_IO_MODE bit 6 in Register 03H and Primary/Secondary enables in Register 04H bits 3, 2, 1, and 0 are globally enabled based on the values written into Register 2D and the Host writing into the configuration index bits in CCR0.

EN_MEM_MODE bit 0 and the EN_INDP_MODE bit 1 in Register 03H are globally enabled based on the values written into Register 2EH and the Host writing into the configuration index bits in CCR0.

EEPROM Register

Address: SELECT 2FH
Name: Bus Control
Type: Read/Write

Bit Placement	Bit Name	Description
Bit 0	EN_BHE_POL	When this bit is cleared, it enables the polarity of the ATA_BHE output to be active High. When it is set, it enables the polarity to be active Low. At Power-On Reset, this bit defaults to clear. Also see Register 00H.
Bit 1	EN_16_DUECE	When this bit is set, it enables word-to-byte access when in memory mode. This mode allows a 16-bit host to access 8-bit peripherals. When cleared, this bit disables word-to-byte access mode. When set, this bit enables the 017 to generate two peripheral write or read strobes on the local peripheral side when the host writes or reads 16 bits of data. This mode allows a 16-bit host to read/write to 8-bit peripheral device registers with one 16-bit access. When this mode is enabled, and the 017 is in memory mode, the host can access the peripheral's 8-bit registers by selecting an even address using PC_HCE1. The 017 asserts the /PC_WAIT pin, which allows the write or read strobe to the peripheral device to be controlled through the "DUECE_WIDTH" and "DUECE_ACCESS_DLY" bits in the Bus control Register 2FH and the externals peripherals IOCHRDY signal if present (Figure 3-1). PCMCIA to local peripheral data path information is shown in Figure 3-2.
Bit 2	EN_DIV_ADDR	When set, this bit indicates that PCMCIA host address lines A3, A2 and A1 are mapped to the local interface address lines A2, A1 and A0. When cleared, PCMCIA address lines A2, A1 and A0 are mapped to local interface A2, A1 and A0.
Bit 3	EN_MAP_IO_MEM	When this bit is set, all memory accesses are mapped to ATA_HIOR and ATA_HIOW. When it is cleared, all memory accesses are mapped to ATA_MRD and ATA_MWR.
Bit 5-4	DUECE_WIDTH	These bits set the /ATA_HIOR/HIOW strobe width and are clocked by PC_MCLK_IN /2. At Power-On Reset, they default to 00.
Bit 7-6	DUECE_ACCESS_DLY	These bits set the /ATA_HIOR/HIOW access delay and are clocked by PC_MCLK_IN /2. At Power-On Reset, they default to 00.

The /ATA_HIOR/HIOW strobe width is three cycles minimum (PC_MCLK_IN /2), plus IOCHRDY time (if any), plus width count programmed in bits 5, 4 (Table 3-14).

Table 3-14. Strobe Width and Access Delay*

Bits						Bits					
7	**6**	**5**	**4**	**Delay**	**Width**	**7**	**6**	**5**	**4**	**Delay**	**Width**
0	0	0	0	0	0	1	0	0	0	2	0
0	0	0	1	0	1	1	0	0	1	2	1
0	0	1	0	0	2	1	0	1	0	2	2
0	0	1	1	0	3	1	0	1	1	2	3
0	1	0	0	1	0	1	1	0	0	3	0
0	1	0	1	1	1	1	1	0	1	3	1
0	1	1	0	1	2	1	1	1	0	3	2
0	1	1	1	1	3	1	1	1	1	3	3

Note: * Each count equals PC_MCLK_IN /2

3.3 WORD-TO-BYTE OPERATION

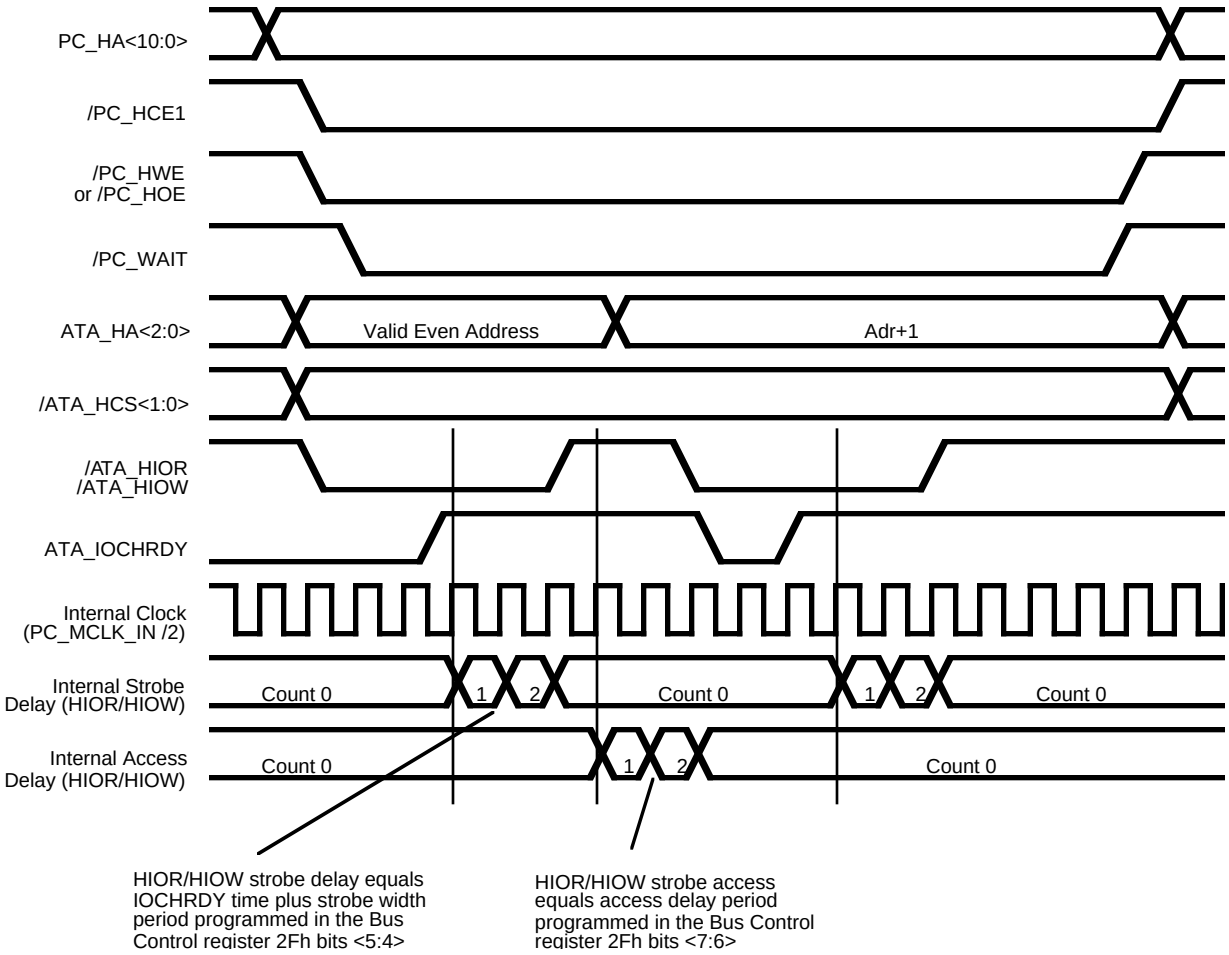

Figure 3-1. Word-to-Byte Timing

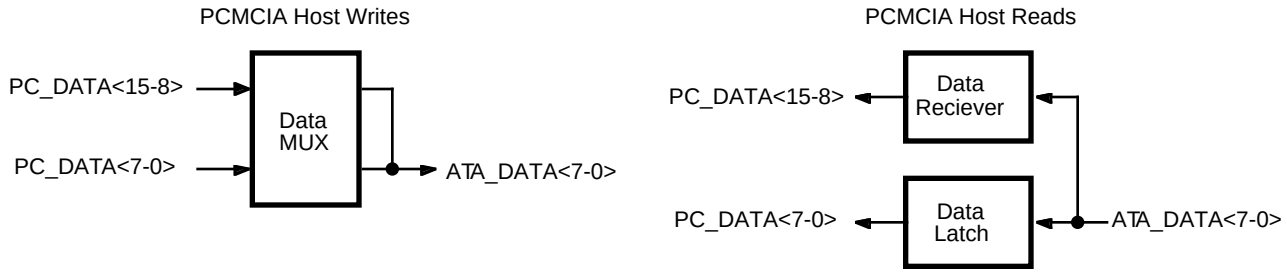

Figure 3-2. Word-to-Byte Mode Data Path

PCMCIA Host Write

PC_DATA<7–0> (Even Byte) Written to ATA_DATA<7–0>
PC_DATA<15–8> (Odd Byte) Written to ATA_DATA<7–0>

PCMCIA Host Read

The PCMCIA selects an even address, then the 017 pulls WAIT and reads the even register from the peripheral device, saves it in a latch, increments the local peripherals address bus, then reads the odd data byte and clears the PCMCIA WAIT pin.

ATA_DATA<7–0> (Even Byte) put onto PC_DATA<7–0>
ATA_DATA<7–0> (Odd Byte) put onto PC_DATA<15–8>

Table 3-15. PCMICA Host Read and Write Address Examples

PCMCIA ATA/IDE Memory Mode		General-Purpose Maps	
Host Address 0	Word Access Only	Host Address 0	Peripheral Address 0, then 1
Host Address 2	Peripheral Address 2, then 3	Host Address 2	Peripheral Address 2, then 3
Host Address 4	Peripheral Address 4, then 5	Host Address 4	Peripheral Address 4, then 5, and so on.

Notes:
1. If the peripheral asserts the /ATA_IOCS16, then this feature will be aborted.
2.The host accesses must be on even addresses.